

ALP280

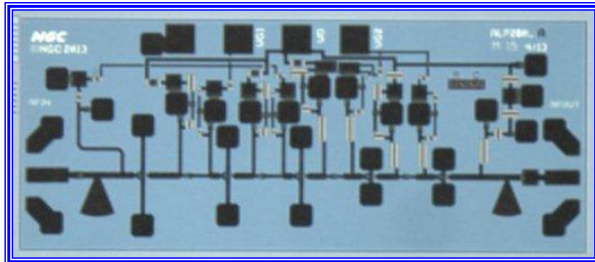
80-100 GHz

Low Noise Amplifier

NORTHROP GRUMMAN

Product Datasheet

Revision: April 2014



X = 2.0mm Y = 0.85mm

Product Features

- RF frequency: 80-100 GHz
- Broadband Operation
- Linear gain: 29 dB, typical
- Noise Figure: 2 dB, typical
- P1dB : 3 dBm *
- Microstrip Topology MMIC, In-line Input & Output
- 0.1 um InP HEMT Process
- 3 mil substrate
- DC Power: < 35 mW
- Die Size 1.7 sq. mm

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	80		100	GHz
Linear Gain	25	29		dB
Input Return Loss	4	10		dB
Output Return Loss	5	12		dB
Noise Figure		2	3.5	dB
Noise Figure (Ave.)		2.6	3	dB
P1dB *		3		dBm
Vd		1.3		V
Vg1=Vg2		-0.1		V
Id1		25.5		mA

Applications

- W-Band Imaging
- Sensors
- Radar
- Short Haul / High Capacity Links
- W-Band Communication Links

Product Description

The ALP280 W-band InP HEMT Low Noise Amplifier is a 5-Stage, broadband, ultra low noise amplifier MMIC. It can be used in applications such as W-band Imaging, Radar, commercial digital microwave radios and wireless LANs. The small die size allows for extremely compact packaging. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Ti/Au, which is compatible with conventional die attach, thermocompression and thermosonic wire bonding assembly techniques.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Min	Max	Unit
Vd1		1.3	V
Vg1, vg2	-1	0.4	V
Id2		25.5	mA
Input Drive Level *		-24	dBm
Assy. Temperature		150	deg. C

* Estimated

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Page 1

ALP280

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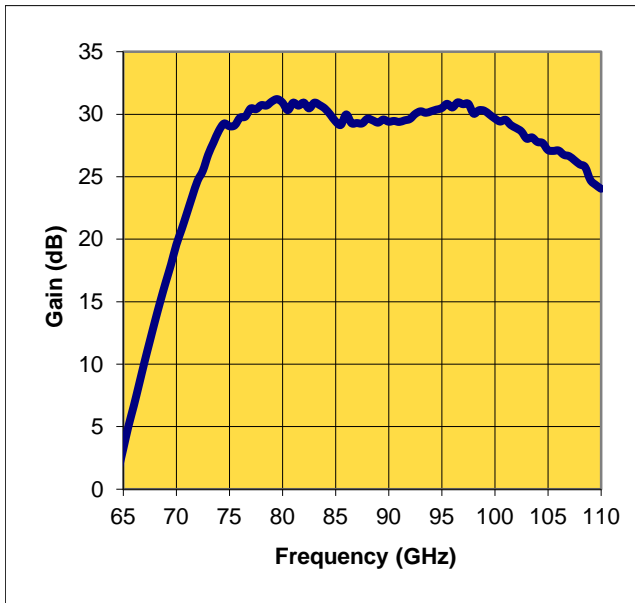
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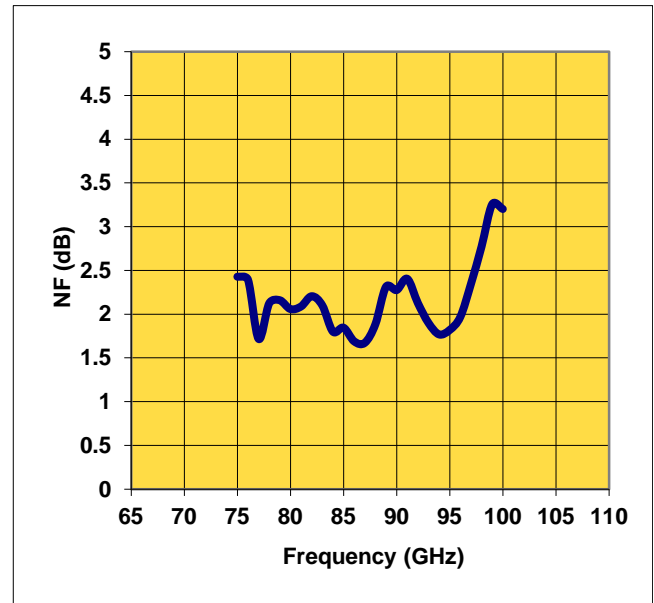
Measured Performance Characteristics (Typical Performance at 25°C)

V_d = 1.3 V, I_d = 25.5 mA* - Wideband Performance

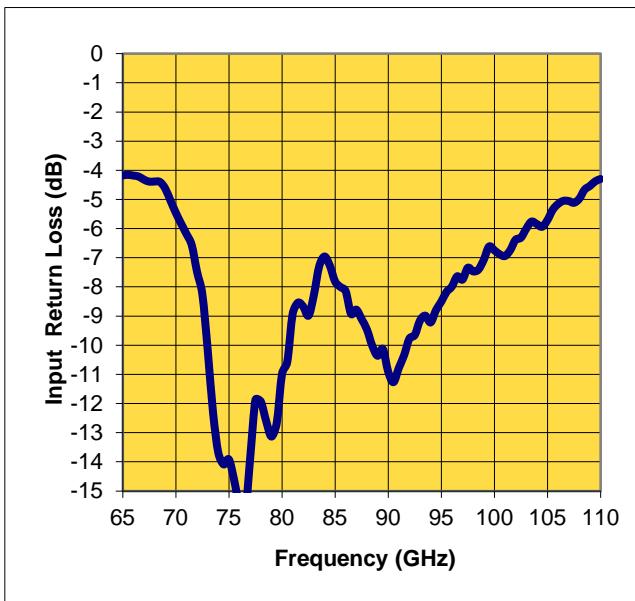
Linear Gain vs. Frequency



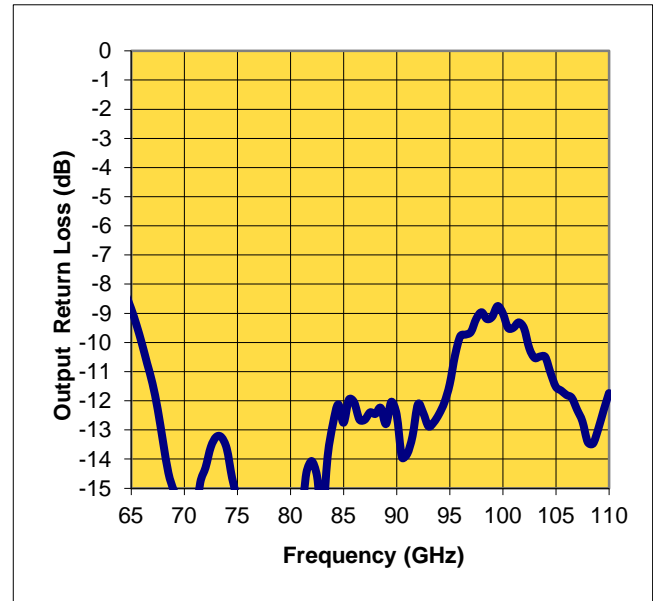
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer, V_{g1}=V_{g2}

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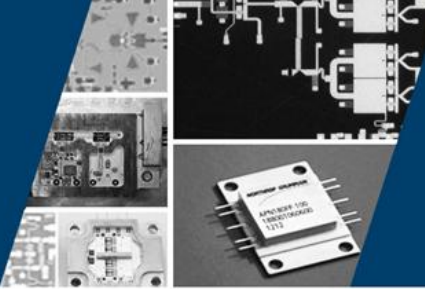
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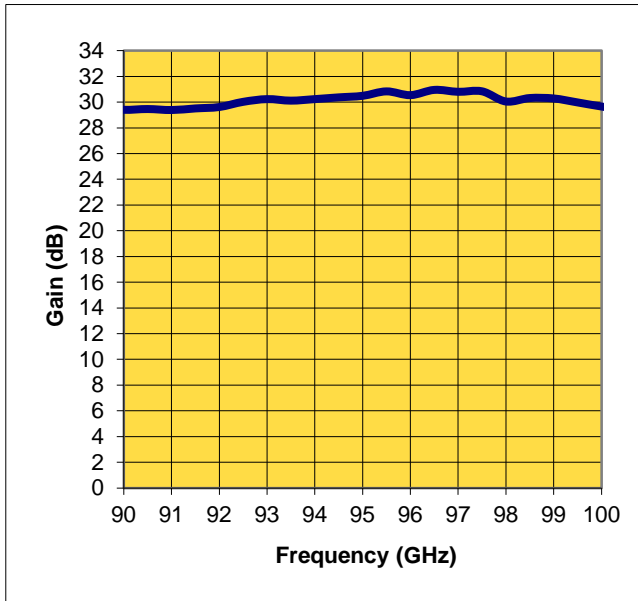
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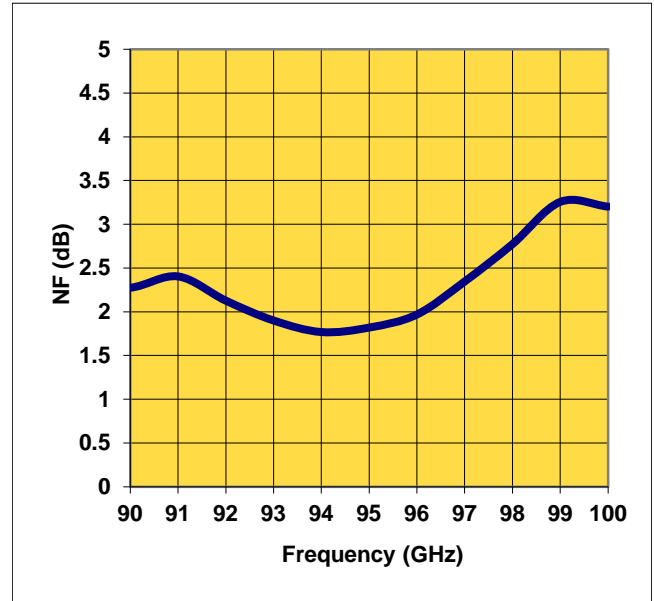
Measured Performance Characteristics (Typical Performance at 25°C)

V_d = 1.3 V, I_d = 25.5 mA* - Performance from 90 GHz to 100 GHz

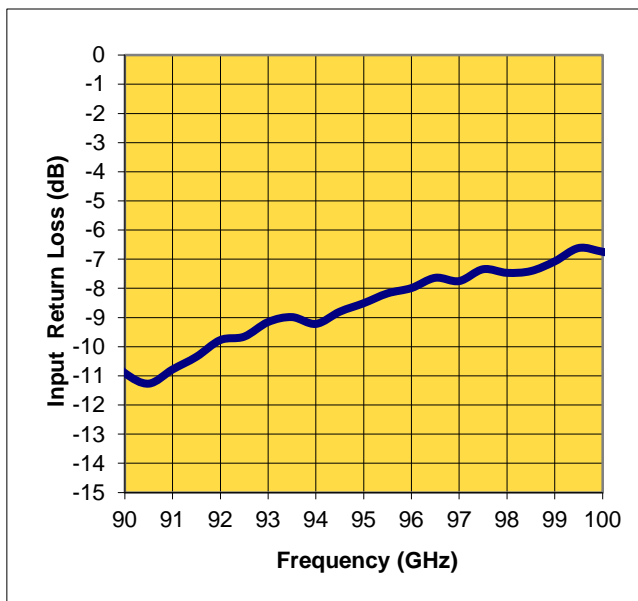
Linear Gain vs. Frequency



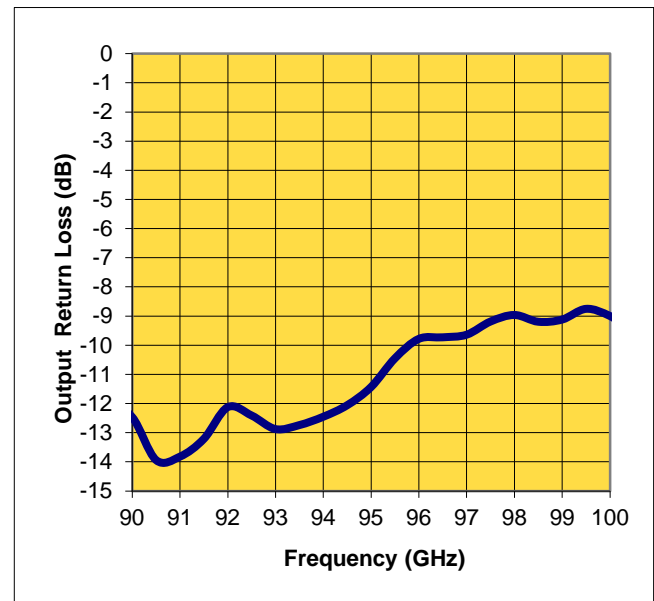
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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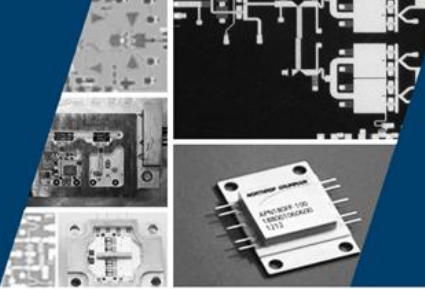
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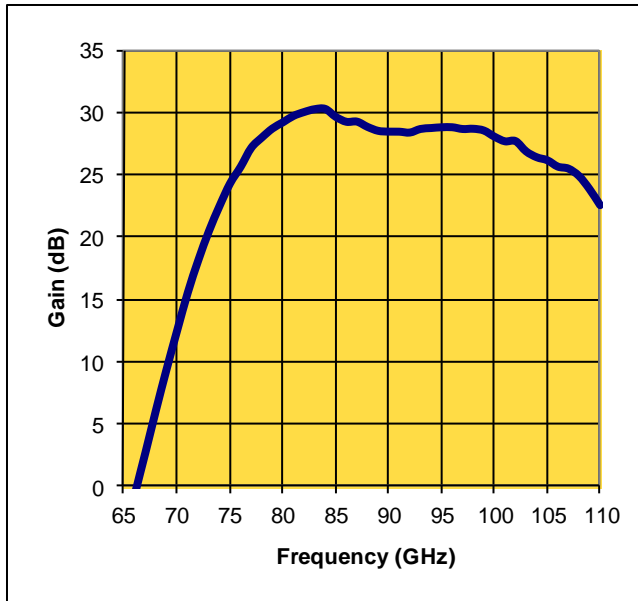
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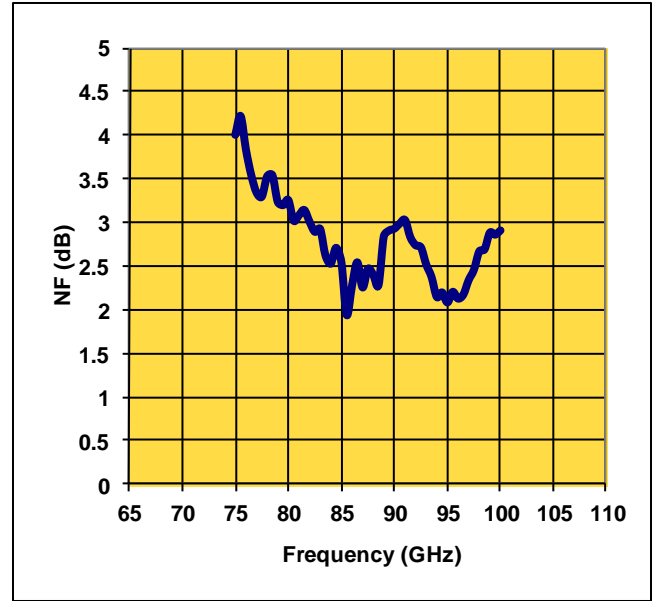
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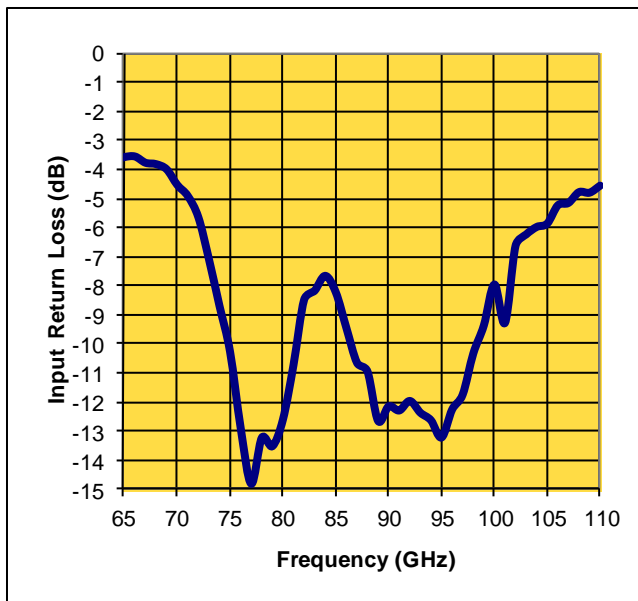
Linear Gain vs. Frequency



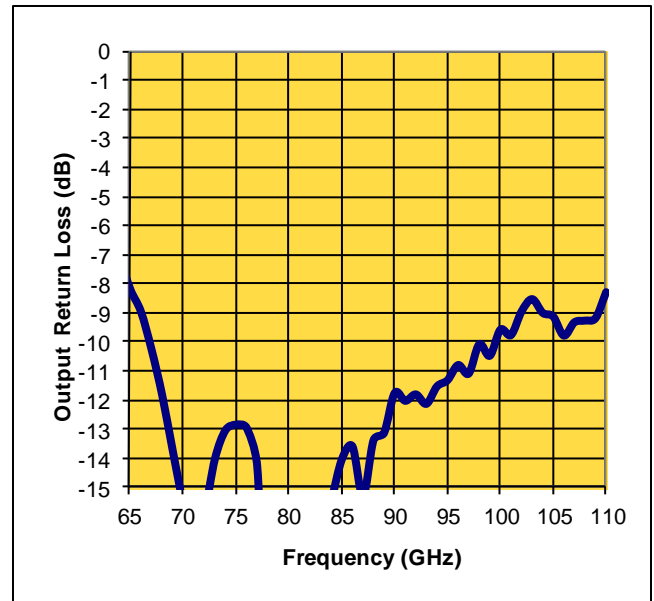
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer, V_{g1} & V_{g2} biased Independently

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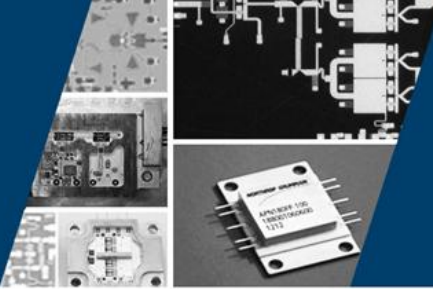
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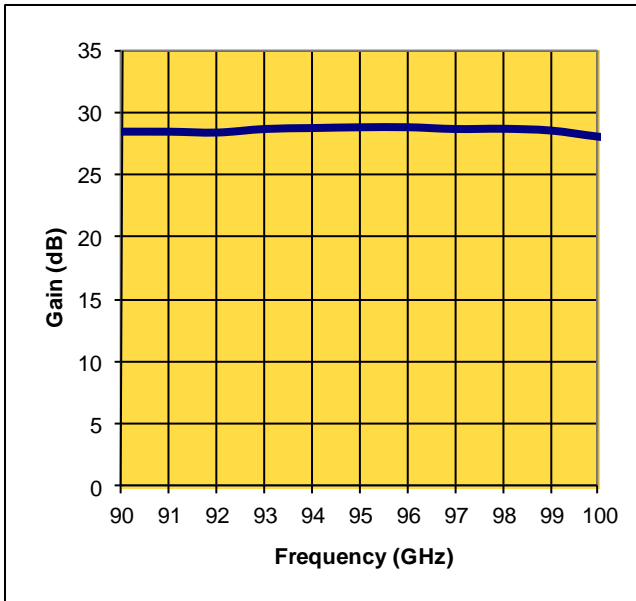
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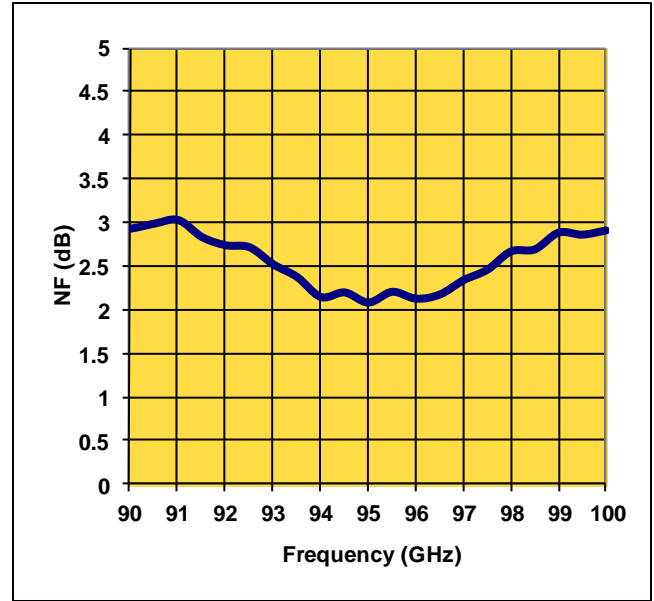
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Measured Performance Characteristics (Typical Performance at 25°C)
 $V_d = 1.3\text{ V}$, $I_d = 25.5\text{ mA}^{**}$ - Performance from 90 GHz to 100 GHz

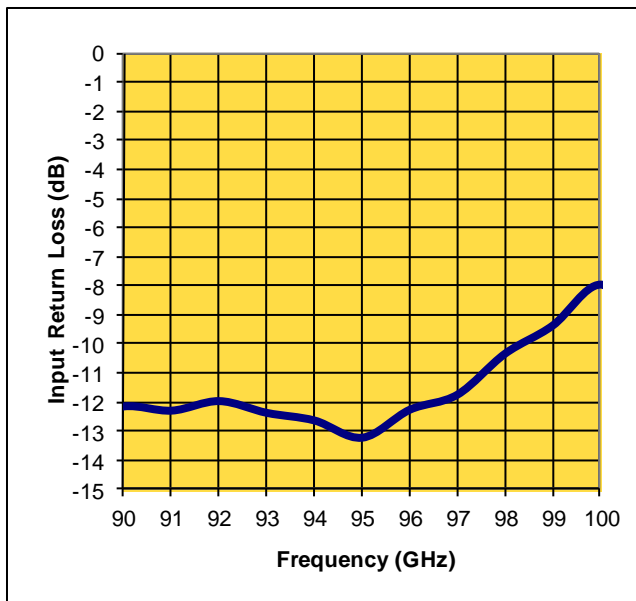
Linear Gain vs. Frequency



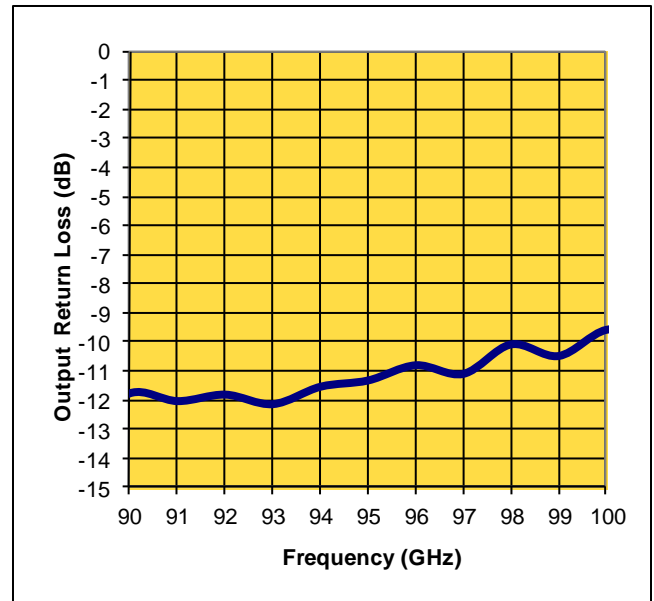
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer, V_{g1} & V_{g2} biased Independently

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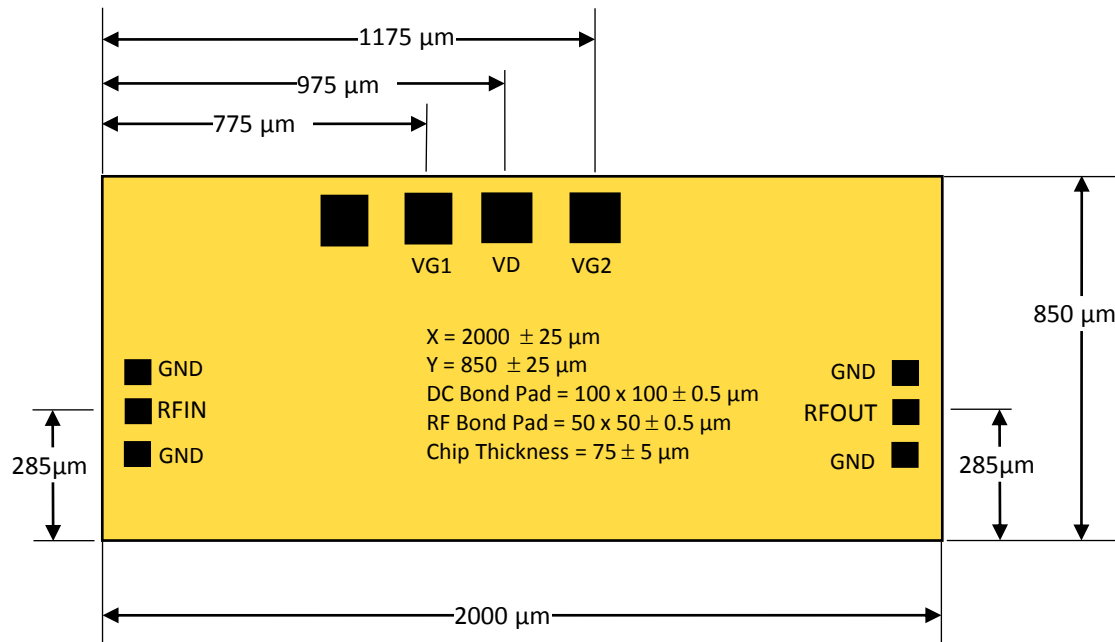
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Die Size and Bond Pad Locations (Not to Scale)



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of < 6 mil (long) by 1.5 by 0.5 mil ribbons on input and output.

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Page 6

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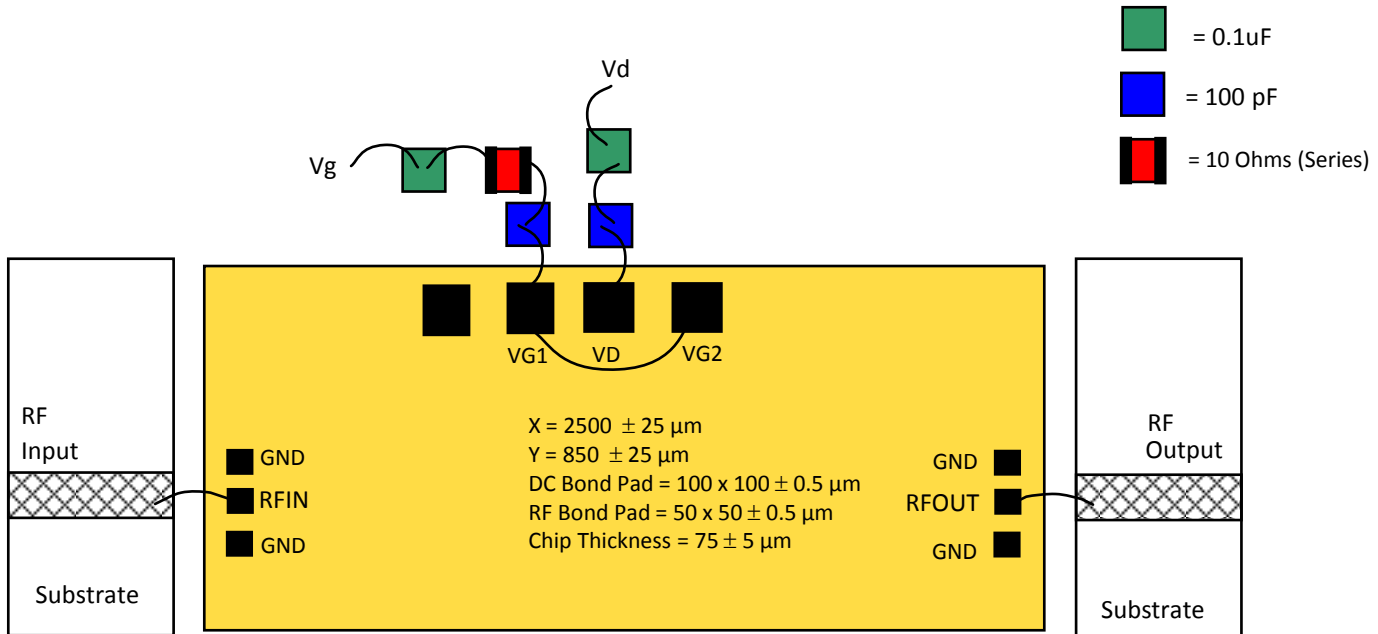
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Suggested Bonding Arrangement



Biasing/De-Biasing Details:

Bias up sequence:

Pinch-off the device by setting $V_{g1} = V_{g2} = -0.6$ and $V_d = 0V$

Increase V_d to the desired value

Adjust $V_{g1}=V_{g2}$ to realize the desired I_d (Nominal Current for I_d for $V_{g1} = V_{g2}$ biased on is 25.5 mA)

Bias down sequence:

Reduce $V_{g1}=V_{g2}$ down to -0.6V

Lower V_d to 0V

Lower $V_{g1}=V_{g2}$ to 0V

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Page 7

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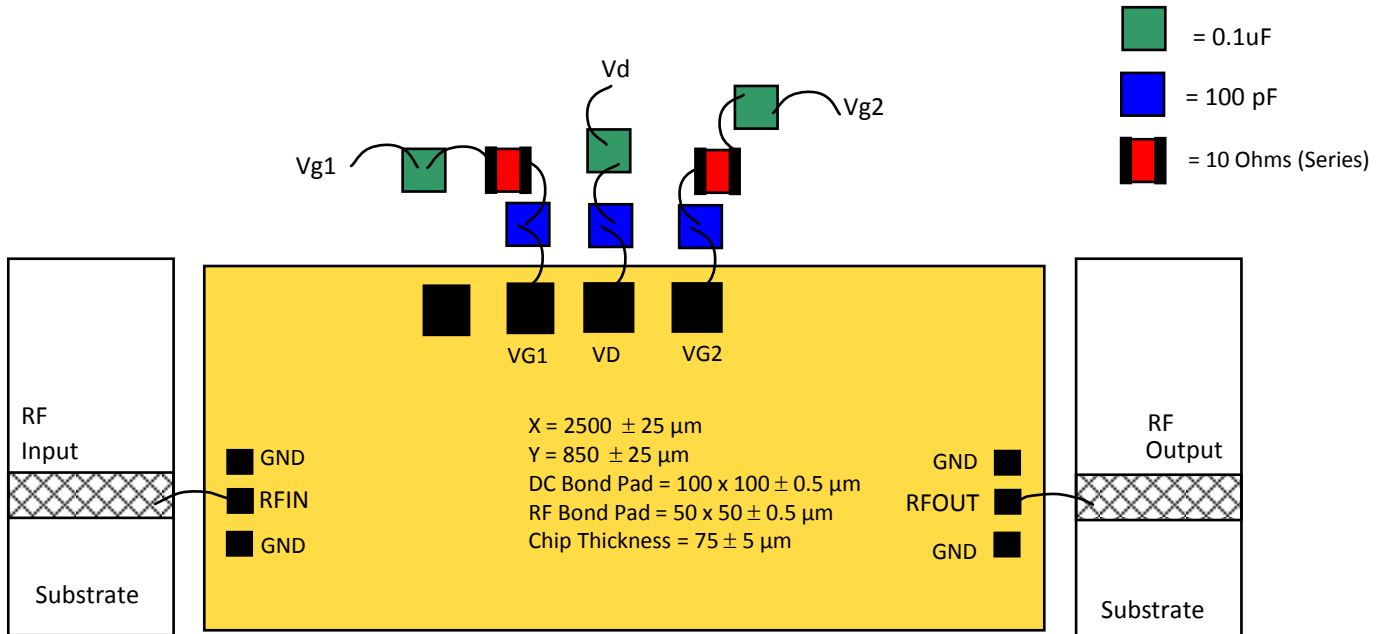
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Suggested Bonding Arrangement (Alternate Bias)



Biasing/De-Biasing Details:

Bias up sequence:

Pinch-off the device by setting $V_{g1} = V_{g2} = -0.6$ and $V_d = 0V$

Increase V_d to the desired value

Adjust V_{g1} to realize the desired I_d (Nominal Current for I_d for V_{g1} biased on is 13.5 mA)

Adjust V_{g2} to realize the desired I_d (Nominal Current for I_d for both V_{g1} and V_{g2} biased on is 25.5 mA)

Bias down sequence:

Reduce V_{g2} down to -0.6V

Reduce V_{g1} down to -0.6V

Lower V_d to 0V

Lower V_{g1} and V_{g2} to 0V

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