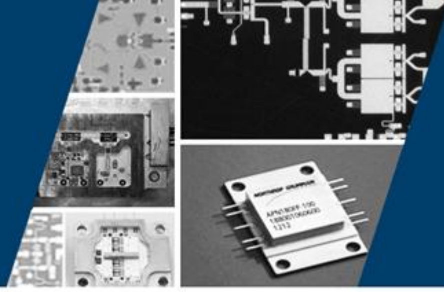
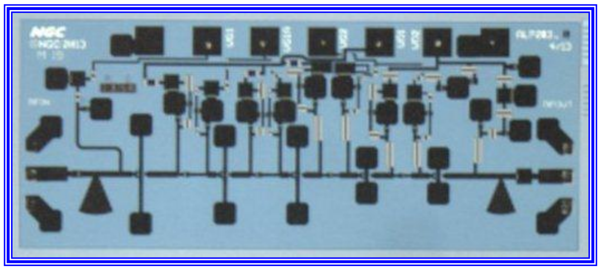
ALP283
80-100 GHz
Low Noise Amplifier



NORTHROP GRUMMAN

Product Datasheet

Revision: May 2014



X = 2.0mm Y = 0.85mm

Product Features

- RF frequency: 80-100 GHz
- Broadband Operation
- Linear gain: 29 dB, typical
- Noise Figure: 2.5 dB, typical
- Average NF (80-100 GHz): 2.1 dB, typical
- P1dB : 3 dBm (Est.)
- Microstrip Topology MMIC, In-line Input & Output
- 0.1 um InP HEMT Process
- 3 mil substrate
- DC Power: < 35 mW
- Die Size 1.7 sq. mm

Applications

- W-Band Imaging
- Sensors
- Radar
- Short Haul / High Capacity Links
- W-Band Communication Links

Product Description

The ALP283 W-band InP HEMT Low Noise Amplifier is a 5-Stage, broadband, ultra low noise amplifier MMIC. It can be used in applications such as W-band Imaging, Radar, commercial digital microwave radios and wireless LANs. The small die size allows for extremely compact packaging. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Ti/Au, which is compatible with conventional die attach, thermocompression and thermosonic wire bonding assembly techniques.

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	80		100	GHz
Linear Gain	25	29		dB
Input Return Loss	4	8		dB
Output Return Loss	7	13		dB
Noise Figure		2.5	3.5	dB
Noise Figure (Ave.)		2.1	2.5	dB
P1dB *		3		dBm
Vd1, Vd2		1.3		V
Vg1		-0.1		V
Vg1a		-0.1		V
Vg2		-0.1		V
Id1		13.5		mA
Id2		12		mA

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Min	Max	Unit
Vd1, Vd2		1.3	V
Vg1, Vg1a. Vg2	-1	0.4	V
Id1		13.5	mA
Id2		12	mA
Input Drive Level *		-24	dBm
Assy. Temperature		150	deg. C

* Estimated

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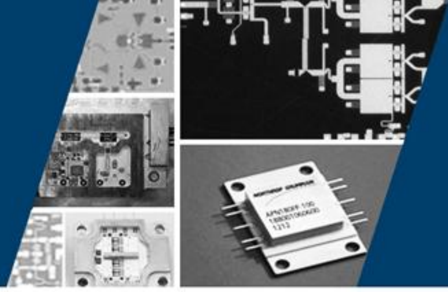
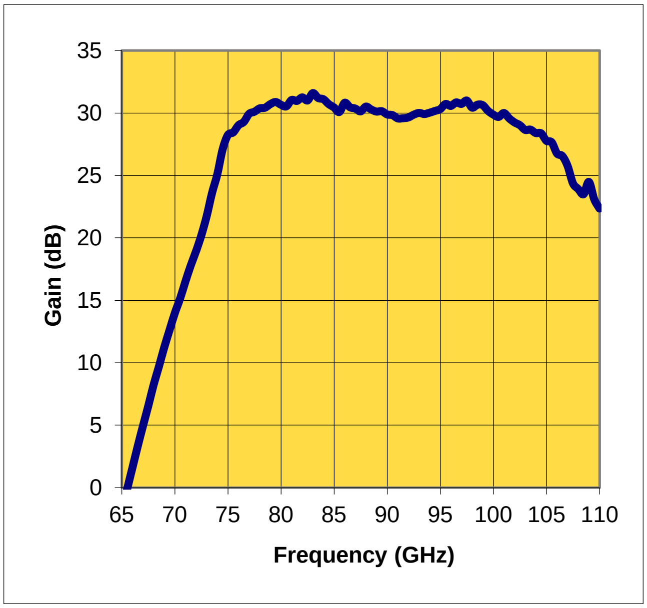
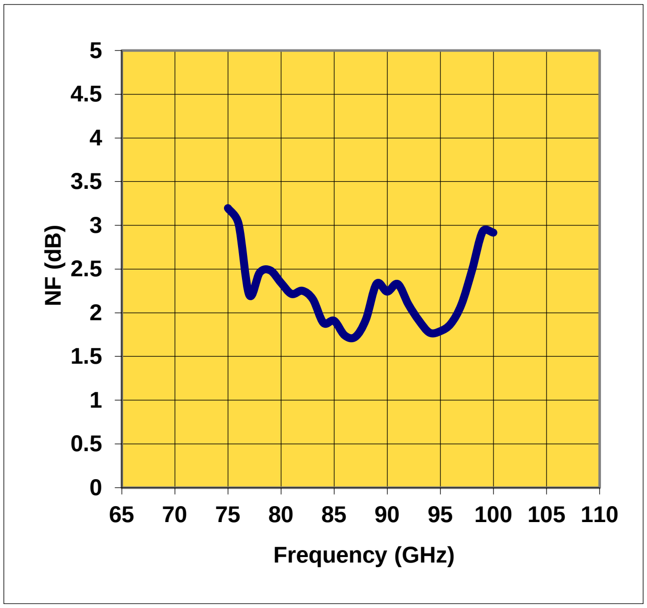


Measured Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd2 = 1.3 V, Id1 = 13.5 mA, Id2 = 12 mA* - Wideband Performance

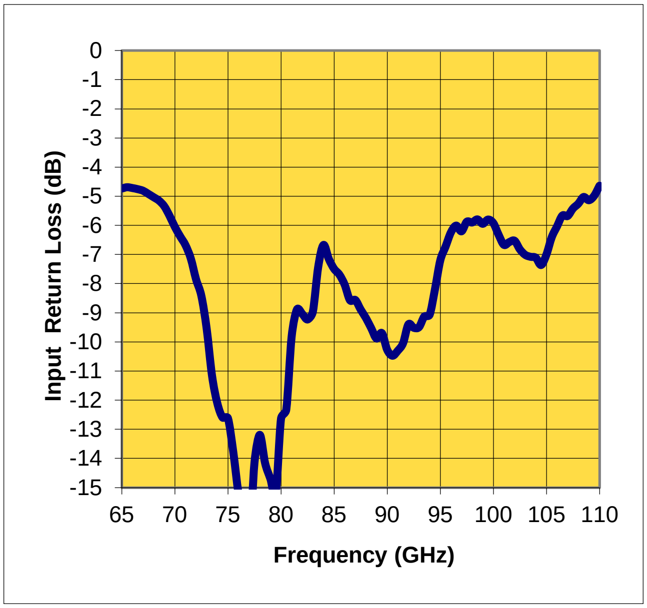
Linear Gain vs. Frequency



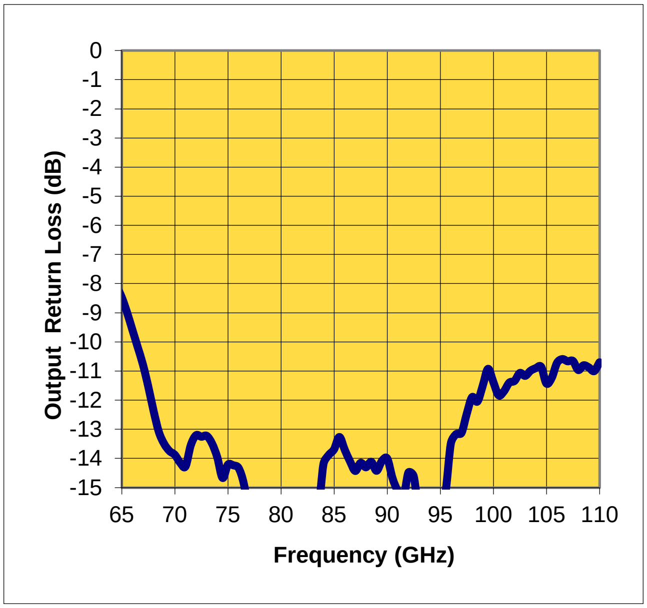
Noise Figure vs. Frequency



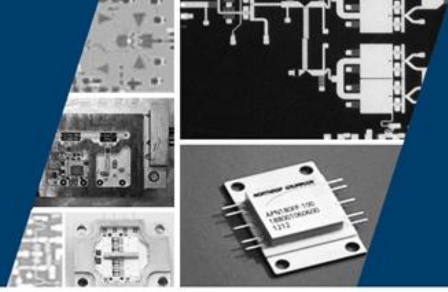
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

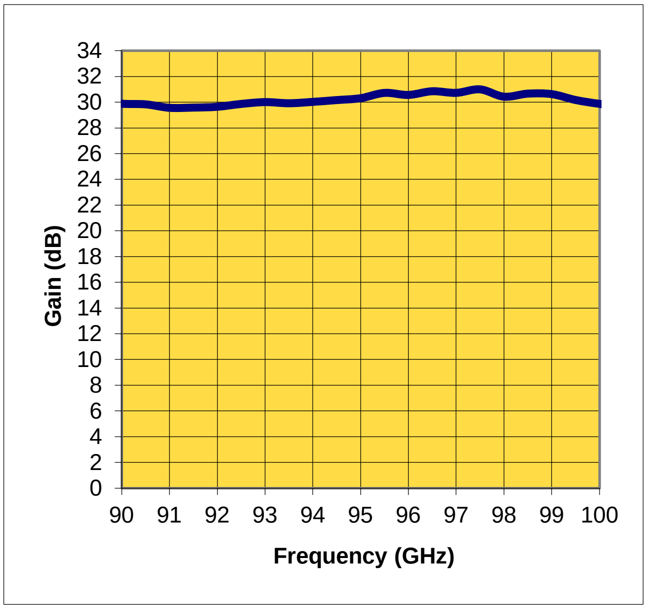


* On-Wafer

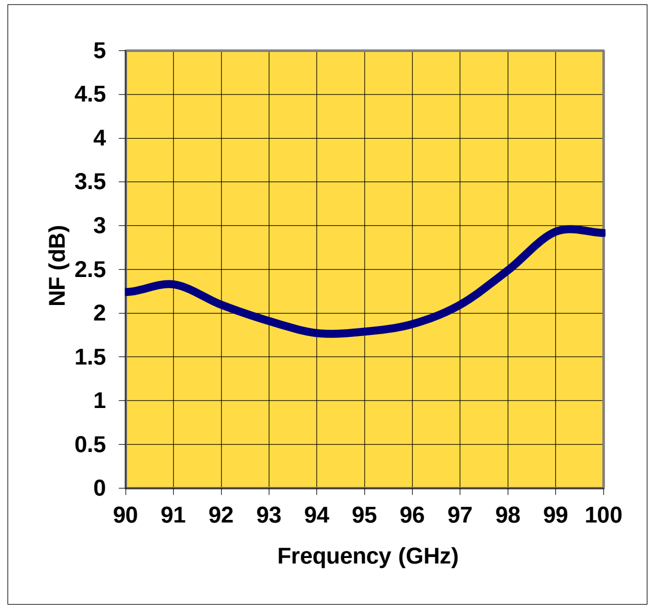


Measured Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd2 = 1.3 V, Id1 = 13.5 mA, Id2 = 12 mA* - Performance from 90 GHz to 100 GHz

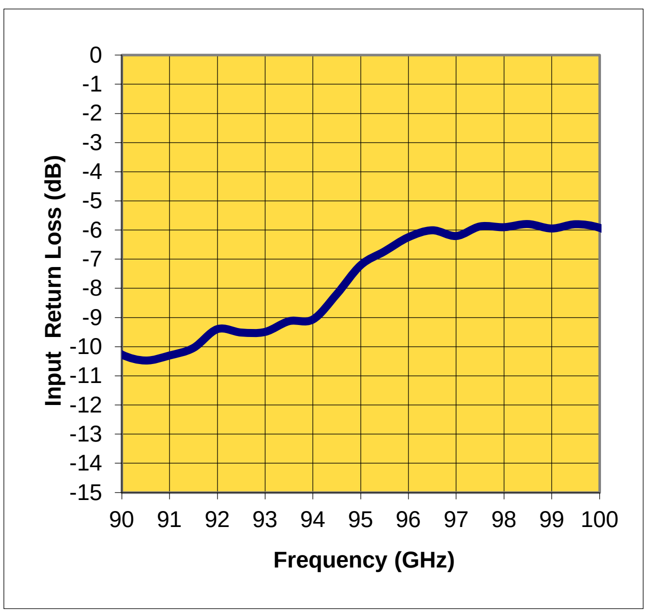
Linear Gain vs. Frequency



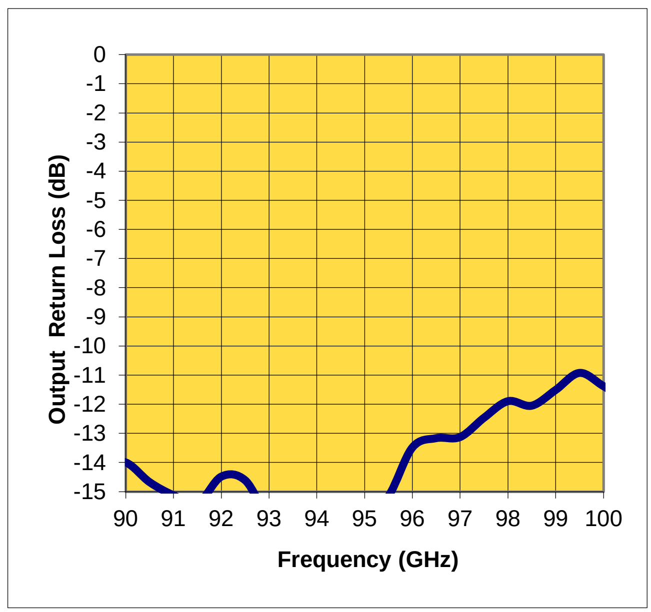
Noise Figure vs. Frequency



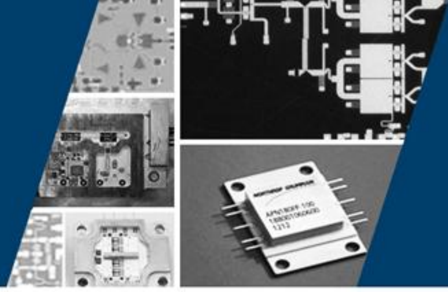
Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer

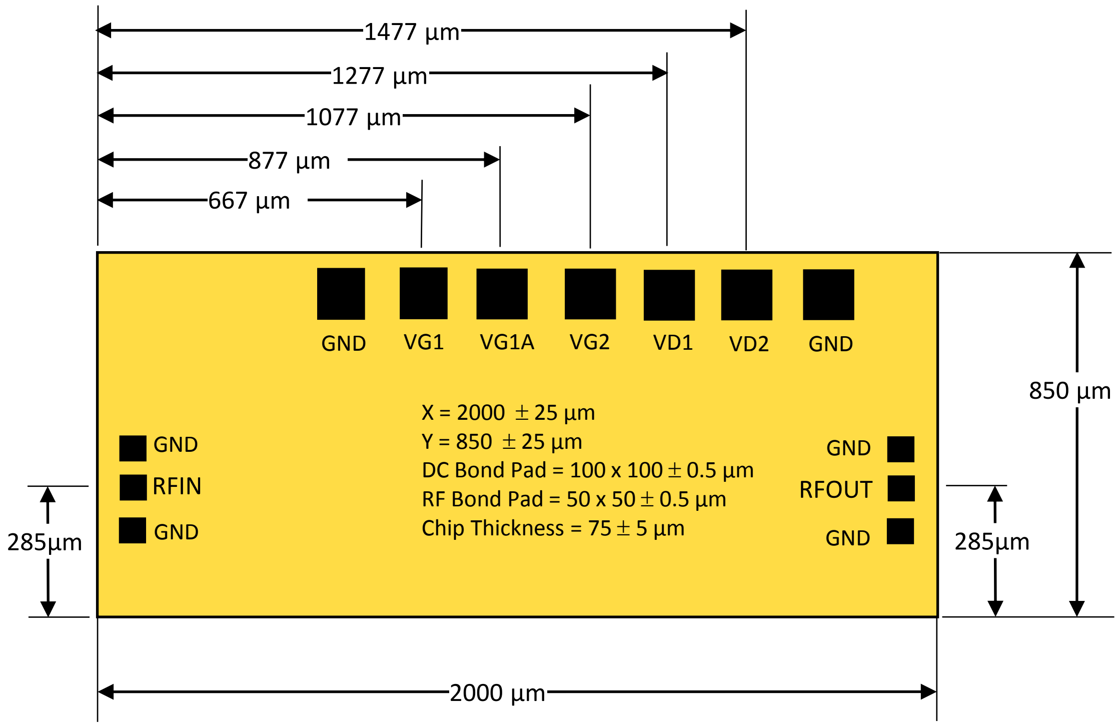


Measured Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd2 = 1.3 V, Id1 = 13.5 mA, Id2 = 12 mA*

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
80.0	0.302	172.470	32.361	-30.366	0.007	76.015	0.091	147.718
80.5	0.298	173.921	31.711	-42.641	0.006	75.951	0.100	145.656
81.0	0.370	170.305	34.056	-53.042	0.009	70.157	0.151	133.913
81.5	0.397	158.261	33.129	-66.809	0.009	58.278	0.181	116.308
82.0	0.385	150.855	33.978	-78.830	0.008	50.717	0.189	102.280
82.5	0.364	148.232	32.641	-91.406	0.008	42.486	0.183	89.634
83.0	0.389	147.364	34.551	-102.020	0.008	44.331	0.160	83.885
83.5	0.453	141.877	33.121	-113.781	0.006	49.092	0.159	92.126
84.0	0.471	128.945	32.233	-125.087	0.008	66.560	0.189	81.304
84.5	0.425	117.400	30.668	-136.037	0.011	58.042	0.183	71.257
85.0	0.410	113.420	29.335	-144.657	0.010	47.667	0.194	70.500
85.5	0.403	104.779	28.543	-153.442	0.008	53.928	0.220	60.440
86.0	0.368	100.086	30.059	-162.833	0.008	41.557	0.201	48.515
86.5	0.350	98.189	28.458	-172.049	0.007	30.829	0.181	46.701
87.0	0.341	92.782	27.979	178.864	0.007	39.707	0.185	49.130
87.5	0.328	91.603	27.360	172.459	0.009	27.899	0.193	40.070
88.0	0.315	84.891	28.408	164.484	0.009	37.298	0.195	32.599
88.5	0.311	81.281	27.749	156.288	0.007	42.400	0.214	19.365
89.0	0.322	79.481	27.601	148.337	0.008	24.473	0.193	17.151
89.5	0.320	73.957	28.571	141.245	0.009	26.458	0.192	8.917
90.0	0.322	64.713	28.493	133.747	0.007	34.261	0.197	-7.179
90.5	0.328	58.225	29.080	125.972	0.005	25.632	0.176	-13.691
91.0	0.331	55.235	28.694	116.828	0.005	28.634	0.155	-15.938
91.5	0.347	48.774	28.995	108.614	0.007	39.779	0.150	-19.586
92.0	0.361	40.022	29.716	100.446	0.007	48.162	0.174	-23.307
92.5	0.353	30.832	30.356	91.608	0.008	47.968	0.165	-40.552
93.0	0.358	25.883	31.147	83.109	0.007	44.762	0.140	-42.768
93.5	0.369	19.746	31.121	74.177	0.009	54.437	0.118	-46.008
94.0	0.384	10.650	31.729	65.025	0.009	33.773	0.134	-36.472
94.5	0.408	2.121	32.267	55.238	0.008	39.060	0.142	-43.363
95.0	0.435	-3.730	32.634	45.269	0.011	31.742	0.143	-37.239
95.5	0.451	-13.320	33.106	35.423	0.008	42.738	0.172	-42.415
96.0	0.474	-23.363	32.558	25.635	0.008	32.792	0.208	-51.039
96.5	0.459	-33.195	32.400	14.778	0.010	37.459	0.210	-59.194
97.0	0.456	-38.989	31.820	5.592	0.010	29.005	0.200	-65.486
97.5	0.487	-44.413	32.244	-3.518	0.011	22.546	0.221	-65.950
98.0	0.470	-50.217	30.443	-13.284	0.011	36.966	0.226	-73.727
98.5	0.480	-61.276	30.826	-22.847	0.009	37.174	0.212	-83.318
99.0	0.470	-64.910	30.805	-33.221	0.010	41.971	0.218	-80.819
99.5	0.485	-69.989	29.171	-42.281	0.011	33.074	0.252	-85.886
100.0	0.486	-77.568	28.144	-51.159	0.011	23.777	0.239	-96.154

* On-Wafer

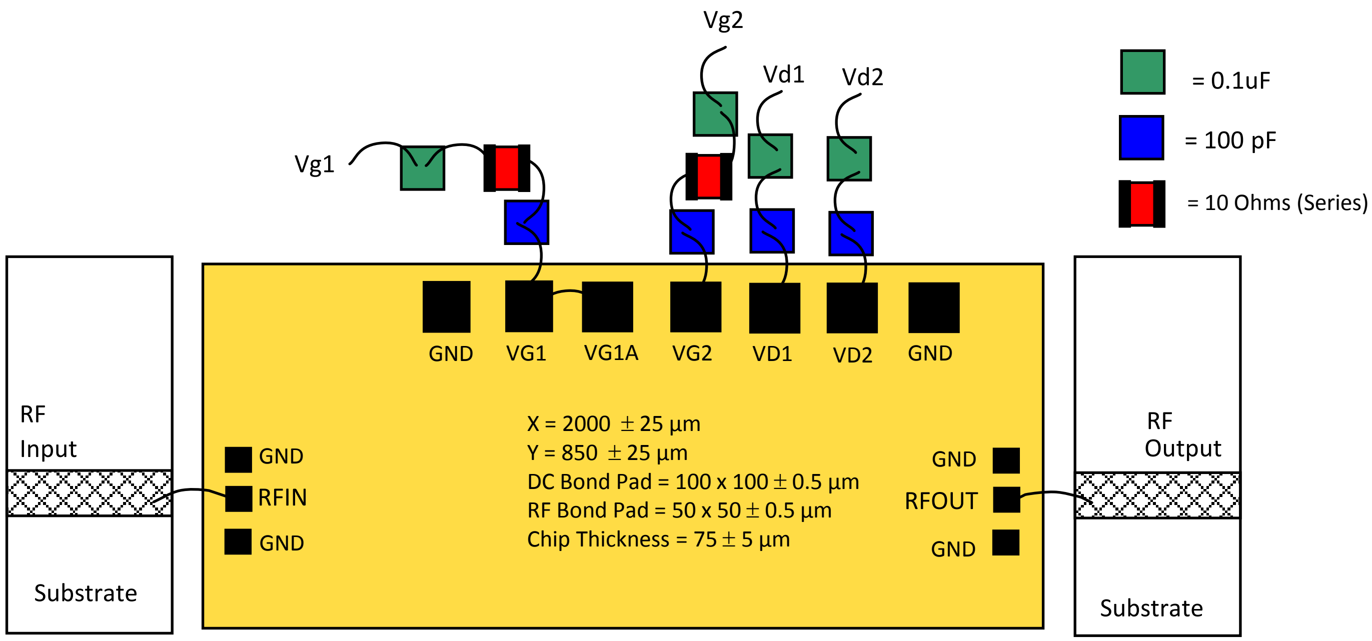
Die Size and Bond Pad Locations (Not to Scale)



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <6 mil (long) by 1.5 by 0.5 mil ribbons on input and output.

Suggested Bonding Arrangement



Biasing/De-Biasing Details:

Bias up sequence:

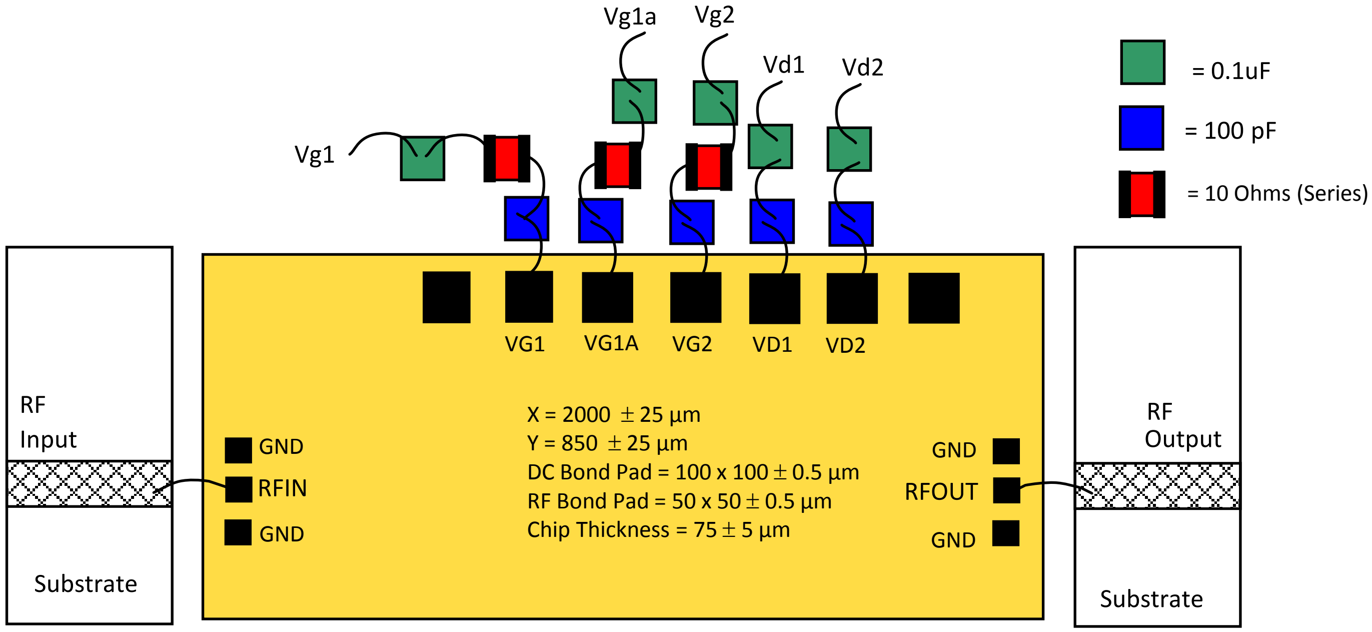
Pinch-off the device by setting Vg1 = Vg1a (Tied together either on or off-chip) & Vg2 to -0.6 and Vd1 & Vd2 to 0V
Increase Vd1 to the desired value (1.3V)
Adjust Vg1=Vg1a to realize the desired Id1 (Nominal Current for Id1 for Vg1=Vg1a biased on is 13.5 mA)
Increase Vd2 to the desired value (1.3V)
Adjust Vg2 to realize the desired Id2 (Nominal Current for Id2 for Vg2 biased on is 12 mA)

Bias down sequence:

Reduce Vg2 down to -0.6V
Reduce Vg1=Vg1a down to -0.6V
Lower Vd2 to 0V
Lower Vd1 to 0V
Lower Vg1 and Vg2 to 0V

Alternate Bonding Arrangement

This configuration allows user to adjust bias to improve the LNAs Noise Figure.



Biasing/De-Biasing Details:

Bias up sequence:

Set Vd1 & Vd2 = 0V
Set Vg1=Vg1a to -0.3V and check to make sure there is no gate current. High gate current indicates leaky devices.
Increase Vd1 to +0.4V and check to make sure there are no oscillations.
If no oscillations are evident, increase Vd1 voltage to recommended value (1.3V).
Adjust Vg1 to realize the desired Id (13.5mA)
Repeat same steps for Vd2.
Set Vg2 to -0.3V and check to make sure there is no gate current .
Increase Vd2 to +0.4V and check to make sure there are no oscillations.
If no oscillations are evident, increase Vd2 voltage to recommended value (1.3V).
Adjust Vg2 to realize the desired Id (12mA)

Bias down sequence:

Reduce Vd2 down to 0V
Reduce Vd1 down to 0V
Set Vg2 to 0V
Set Vg1=Vg1a to 0V