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## **A 256 kb (32kx8) EEPROM for >200 °C Applications**

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**Abstract** – A memory retention study was performed on the W28C256 32kx8 EEPROM device to assess its suitability for use in high temperature applications above 200 °C. This study indicates this device has memory retention in excess of 5 years at 225 °C. During 2014, characterization and extended life testing is planned to further assess device reliability for future high temperature applications.

### I. Background

The Northrop Grumman W28C256 32kx8 256kbit EEPROM is a radiation hardened device that has been used in space applications since 1995<sup>1</sup>. Nonvolatility is achieved using SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) charge storage technology. This design utilizes a four transistor memory cell (compared to a two transistor memory cell used in the W28C0108 128kx8 1Mbit EEPROM). The objective of this study was to evaluate whether the four transistor memory cell and increased programming voltage (10 V vs 7.5 V for the 1 Mbit device) would lead to improved high temperature memory retention.

The EEPROMs evaluated in this study were designed by Sandia National Laboratories in Albuquerque, NM. Fabrication, test, assembly and electrical characterization was performed at Northrop Grumman Corporation in Baltimore, MD. Sandia Technologies Incorporated assisted in the data analysis.

### II. SONOS Nonvolatile Memory Operation

This section will summarize key features of operation for SONOS-based nonvolatile memories. SONOS memories achieve data storage by storing trapped charge in silicon nitride dielectric films. Since

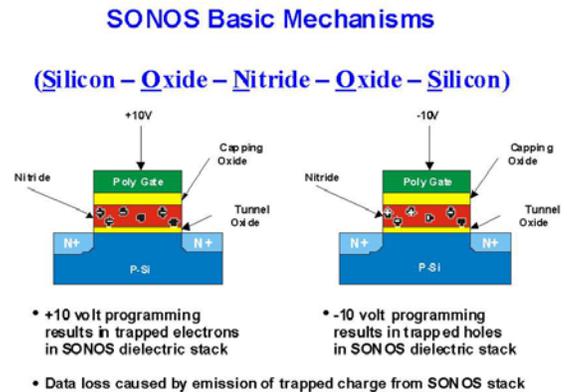


Figure 1. SONOS programming - trapped holes with positive programming and trapped electrons with negative programming.

charge is stored in a dielectric, SONOS memories are less prone to catastrophic memory loss that can occur with floating gate EEPROMs that store charge in a conductive floating gate transistor<sup>2</sup>. Programming is performed under high electric fields with Fowler Nordheim tunneling. The cartoon in Figure 1 shows a simplified view of how programming is achieved. Typical programming voltages are 5 to 10 V and 1 to 100 msec. The memories discussed in this paper use n-channel SONOS transistors. Negative programming creates a high conductance (CLEAR) state. The CLEAR state is strongly depletion mode – ON with zero Volt gate bias that is used during Read. Typical ON currents for the CLEAR state are ~100 uA/um width. Positive programming creates a lower conductance (PROGRAM) state. Sense amplifiers in the memory are able to detect SONOS threshold voltages differences as low as 100 mV. The SONOS memory window is defined as the difference between the CLEAR and PROGRAM threshold voltages.

Memory retention failures will not occur until the memory window drops below 100 mV for the four transistor 256k EEPROM design.

To fully characterize SONOS memory transistors, pulse response and retention curves are generated. This type of testing is used to establish optimal programming conditions for the memory. Figure 2 shows a SONOS pulse response curve. For this measurement, the transistor is programmed into one state (CLEAR or PROGRAM) and then programmed into the opposite memory state with increasingly longer programming pulses. Room temperature 256k EEPROM NSONOS retention data is shown in Figure 3. The memory window is 2.3 V at 10 sec and 1 V when extrapolated out to 10 years. Note that in Figure 3 that the CLEAR (excess hole) state has much lower decay rate than for the PROGRAM (excess electron) state. This is an appealing feature for these NSONOS-based memories since the high conductance CLEAR state

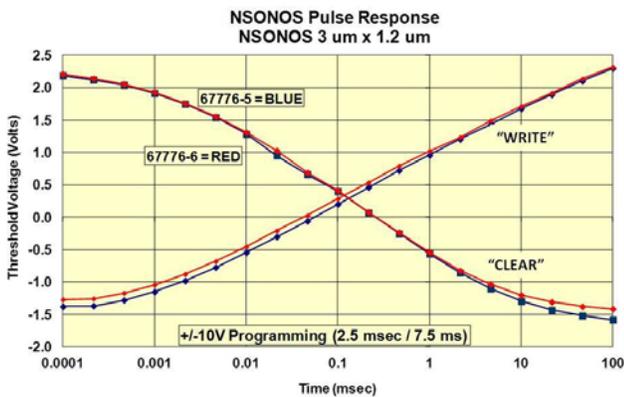


Figure 2. 256k NSONOS pulse response curve is used to select optimum programming conditions.

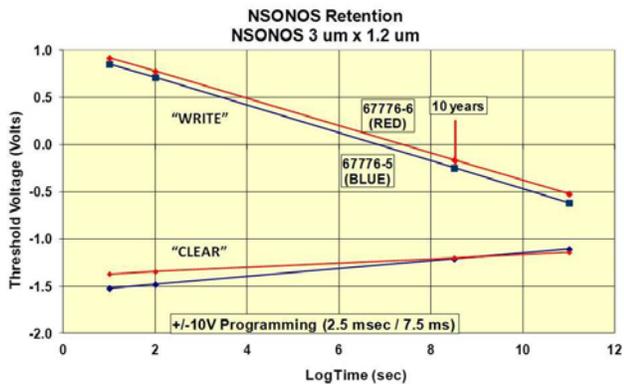


Figure 3. 256k NSONOS retention curve is used to predict retention life time (memory window <100 mV).

changes very gradually during normal part operation. This robust high conductance state enables faster bit line switching and leads to less access time reduction at end of life. To optimize end of life access time, the recommended programming conditions for the 256k EEPROM are - +10 V / 2.5 msec and -10 V / 7.5 msec.

Further retention lifetime improvement can be achieved by using wider pulse widths during programming. This was not evaluated for this investigation. Figure 2 shows that the initial memory window would be increased to ~3.1 V (35% larger) using 10X wider pulse widths (+10 V / 25 msec, -10 V / 75 msec). This is easily done by the user by a 10X change in the clock frequency. This would be of interest in future work since the high temperature applications are more focused on long term retention than reprogrammability.

SONOS memory retention degrades with increasing temperature. At elevated temperatures, charge detrapping rates increase, collapsing the SONOS memory window. Figure 4 shows temperature acceleration effects on retention for the 1Mb EEPROM technology. Data was taken at 125 °C and 250 °C. Note that the memory window after 2 days at 250 °C is equivalent to the memory window after 2600 years at 125 °C. Currently, all 256k and 1M EEPROM product is screened with this 2 day / 250 °C bake to ensure that product will meet 10 year / 125 °C memory retention requirements.

The 256k EEPROM architecture features 512 rows. Each row has 512 columns. Data is read out in 8 bit words so there are a total of 64 unique columns in each row (or page). Figure 5 shows a simplified

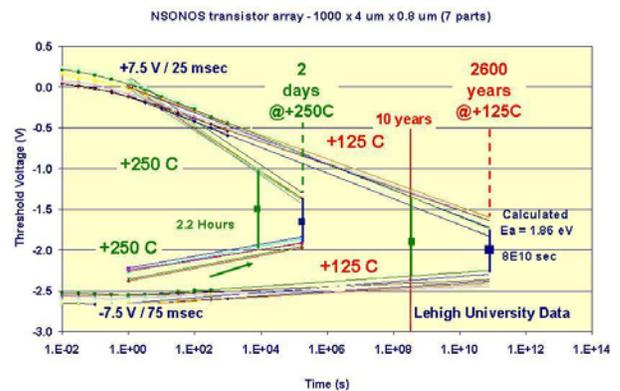


Figure 4. NSONOS retention degradation with increasing temperatures for the W28C0108 128kx8 1Mbit EEPROM.

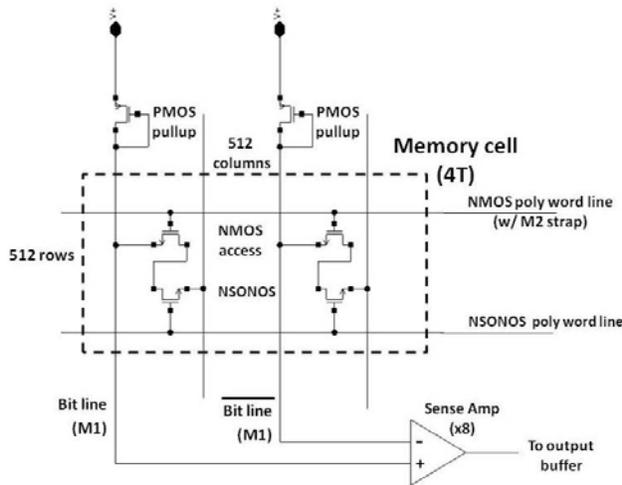


Figure 5. 256k EEPROM four transistor memory cell schematic.

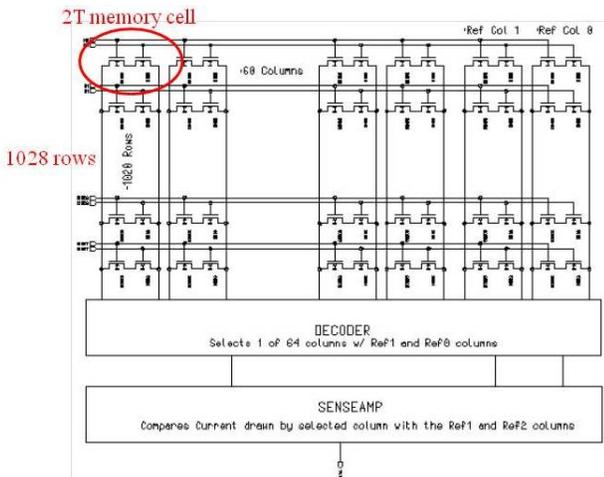


Figure 6. 1M EEPROM two transistor memory cell schematic.

circuit schematic for the 256k EEPROM memory. The 256k EEPROM memory cell has 4 transistors – 2 NMOS pass transistors to connect to the vertical bit lines and two NSONOS transistors to store two complementary logic states (CLEAR/PROGRAM). Reading is performed 8 bits at a time using 8 sense amplifiers at the bottom of the memory cell array. Memory cell state is determined by sensing the difference in voltage levels on the complementary vertical bit lines in the 256k EEPROM memory. When a memory cell is being read, PMOS pull up transistors are connected in series with the access and memory transistors to create either a positive (CLEAR state – “Logic 0”) or negative (PROGRAM

state – “Logic 1”) voltage difference depending on the logic state of the memory cell. Bit lines are precharged to be equal potentials prior to reading to speed up the access time for the part.

The 1M EEPROM uses a slightly different detection scheme to achieve higher memory density. Like the 256k EEPROM, it uses a x8 organization with 1024 rows (pages) and 1024 columns (128 columns x 8 bits). However, a two transistor memory cell is used with a single NMOS access transistor and single NSONOS memory transistor per cell (Figure 6). A set of 64 reference memory cells is incorporated that are connected to sense amplifiers to help determine the memory cell state. Each reference cell features a pair of two transistor memory cells – one written to the CLEAR state and one written to the PROGRAM state. This two transistor memory cell with onboard reference cell approach roughly doubles the memory cell density for the 1M EEPROM relative to the 256k EEPROM. During Read, an averaging circuit is used that delivers the average voltage of the reference CLEAR and PROGRAM states to the reference cell bit lines. The 1M EEPROM sense amplifier then detects the difference between the reference cell and the memory cell bit lines. This averaging approach for the 1M EEPROM roughly halves the voltage difference delivered to the sense amplifiers. The purpose of this study was to determine whether the larger voltage difference in the bit line voltages for the 256k EEPROM part would lead to better long term memory retention at elevated temperatures.

### III. 256k EEPROM Memory Retention Data

Cumulative time to retention failure distributions were generated by programming devices with a checkerboard pattern, followed by unbiased exposure to high temperatures, with interval retention testing at room temperature. 256k EEPROM sample sizes varied from 14 to 33 parts. The failure criterion was defined as a single bit failure in a device memory. (This study assessed retention activation energy for the extreme “outlier” bits in each memory part evaluated.) The activation energy was then derived based on the traditional Arrhenius relationship for median time to failure (MTTF);

$$MTTF = A \cdot \exp(E_a/kT) \quad \text{where } E_a \text{ is activation energy, } k = \text{Boltzman's constant and } T = \text{temperature}$$

## 1Mb EEPROM Retention Activation Energy Study

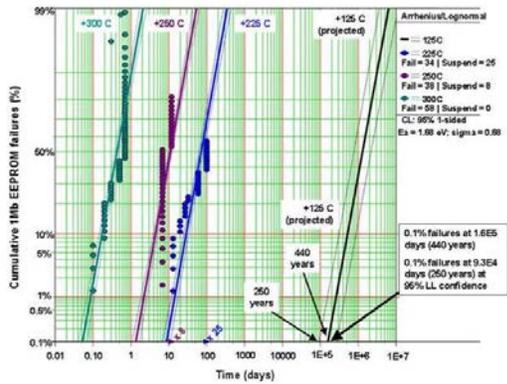


Figure 7. 1M EEPROM retention study from 2008 showed retention life time of >250 years at 125 C.

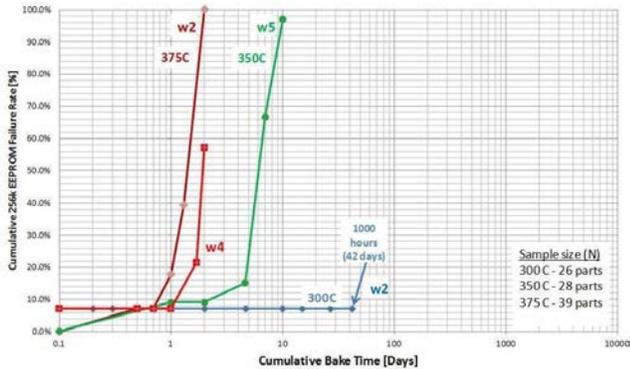


Figure 8. 256k EEPROM retention study from 2014 (this work) had median time to failure of 1.6 days at 375°C, 6 days at 350°C and >42 days at 300°C.

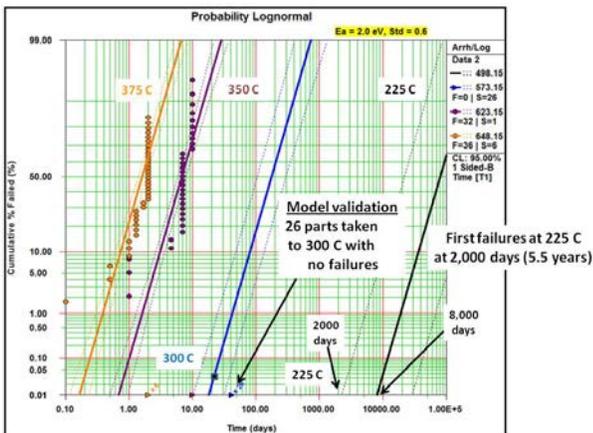


Figure 9. 256k EEPROM retention study from 2014 (this work) shows retention life time of >5 years at 225 °C.

A similar retention study was performed in 2008 on the 1Mbit EEPROM device<sup>3</sup>. Figure 7 shows the overall summary from this study. A memory retention activation energy of 1.68 eV was measured which predicted that first 1 Mbit EEPROM failures would occur at 250 years at 125 °C. In this study, we evaluated the 256k EEPROM as a candidate for high temperature applications because of its more robust memory cell design (4 transistor instead of 2 transistor) and its larger programming voltage (+/-10 V vs +/-7.5 V programming).

The 256k EEPROM MTTFs measured were 1.6 days, 6 days and >42 days at 375, 350 and 300°C, respectively (no failures were seen out to 42 days at 300 °C and testing was suspended). A simplified time to failure summary for this 256k EPROM data set is shown in Figure 8.

The 256k EEPROM retention data was then analyzed using Reliasoft Alta software which performs quantitative analysis of part reliability. Figure 9 shows the Alta software analysis of this 256k EEPROM data with 95% confidence intervals.

The distributions shown in Figure 9 are well behaved and nearly identical at the two stress temperatures. There appears to be an extrinsic tail comprised of roughly 10% of the sample tested. Removal of this tail from the analysis reduces the lognormal sigma from roughly 0.58 to 0.24, resulting in low retention life variability for the main population. The activation energy extracted from the data shown in Figure 8 is 2.0 eV. Removal of the extrinsic population from the activation energy extraction did not change the result. The lower 95% confidence bound at 0.01% cumulative retention life at 225 °C is greater than 5.5 years for the entire sample tested. Because of the presence of an extrinsic population, the current plan is to implement a 1 day / 300 °C screen for high temperature applications which is estimated to be equivalent to 445 days at 225°C.

## IV. High Temperature Characterization

A fixture was built to allow testing of packaged parts at elevated temperatures as high as 300 °C. The high temperature test socket is designed to accept a 40 pin ceramic DIP. All of the materials used to construct the socket have temperature ratings over 400 °C. The socket is zero insertion force and spring pressure is easily applied to the package pins by the use of four

thumb screws. An integral flying-lead cable bundle is used to bring signals in and out of the DUT eliminating the need for any solder joints inside the temperature chamber. Once completed, characterization work will be performed to evaluate changes in AC and DC parameters for the 256K EEPROM at 200, 225 and 250 °C. SPICE simulations are also being done to evaluate the suitability of this part for 200 to 225 °C applications.

Previous qualification work indicated address access times for the W28C256 256k EEPROM were 90/115/155 nsec at -55/+25/+125 °C. This access time is linear with temperature (slope = 0.36 nsec /deg C) so the access time should increase from 155 nsec to ~190 nsec at +225 °C.

SONOS EEPROM access times can degrade as the SONOS memory window collapses due to changes in the response time of the memory cell sense amplifiers. If the SONOS memory window collapses too much, the sense amplifier can take longer to sense the state of the memory cell. In general, this effect is primarily observable at extreme end of life conditions. To evaluate this, parts will be given a 1 day / 300 °C end of life retention bake. Based on this 256k EEPROM retention study, with an activation energy of 2.0 eV, it is estimated that this bake stresses parts to a memory window position equivalent to 445 days at 225 °C. A final access time specification recommendation will be made once this high temperature characterization work is completed.

## V. Part Qualification for >200 C applications

The W28C256 32kx8 256kbit EEPROM has been in production for space applications since 1996. Reliability screening is performed in accordance with MIL-STD-883. This screening includes wafer level retention, dynamic burn in (80 hours, dynamic, 150 °C), high temperature Group C life testing (1,000 hours, dynamic, 150 C), Group A/B/D package tests and Group E total ionizing dose [300 krad(Si) ]. For high reliability applications, the 256k EEPROM parts have also successfully passed 2,000 hour dynamic life testing at 150 °C, 6000 hours memory retention at 150 °C, and 10,000 endurance (program/clear) cycling followed by 1 day / 250 °C “end of life” retention bake. An extended life test was also completed successfully in 2009 with 15 parts passing after 15,000 hours at 150 °C. All of this testing to date has indicated excellent reliability for the 256k

EEPROM part for space and avionics applications. (Over 564,000 equivalent device-hours at 125 °C with no failures) This section will discuss future plans for evaluating this part for high temperature applications above 200 °C.

During the 256k EEPROM memory retention activation energy study, parts were taken to 300 °C for 42 days with no loss in functionality or retention. However, during the testing some hard failures were observed on some die that were exposed to 2 days at 375 C or 10 days at 350 °C. An extended life test at 1000 hours at 250 °C will be performed to verify that this product is suitable for 225 °C applications. The 256k EEPROM part has previously successfully passed latch up testing in both heavy ion and prompt dose test conditions. No latch up was seen with heavy ion linear energy transfer (LET) of 60 MeV-cm\*\*2/mg and flash x-ray dose rate of 1E12 rad(Si)/sec. However, latch up becomes more likely at elevated temperatures (due to increased parasitic bipolar current gain) so this will need to be evaluated again at 225 C during this evaluation phase.

## VI. Summary

The W28C256 32kx8 256kbit EEPROM has been characterized for high temperature memory retention and has estimated retention beyond 5.5 years at 225 °C with an activation energy (Ea) of 2.0 eV. This long term retention may enable users to avoid having to reprogram the EEPROM memory parts during some high temperature applications. The 256k EEPROM part performed better than the 1Mbit EEPROM part for high temperature memory retention. The improved retention for the 256k EEPROM is explained by the more robust 4 transistor memory cell and the increased SONOS memory window in this part. Characterization testing is underway to evaluate part operation and part reliability for applications above 200 °C. High temperature life testing (250 °C) is expected to be complete by the end of 2014.

## References

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