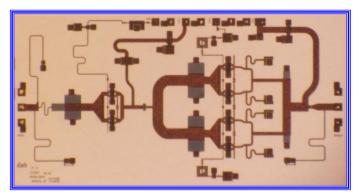
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X = 4.4 mm Y = 2.28 mm

# **Applications**

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

# **Product Description**

The APN149 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, Military SatCom and Radar Applications. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

## **Product Features**

RF frequency: 18 to 23 GHz

■ Linear Gain: 20 dB typ.

Psat: 38 dBm typ.

■ Efficiency @ P3dB > 30 %

■ Die Size: < 10.032 sq. mm.

0.2um GaN HEMT

4 mil SiC substrate

■ DC Power: 28 VDC @ 544 mA

ECCN: 3A611.x

HTS (Schedule B) code: 8542.33.0000

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#### **Absolute Maximum Ratings**

Parameter	Value	Unit	
Drain Voltage	28	V	
Gate Voltage Range	-8 to 0	V	
Drain Current	700	mA	
Gate Current	0.3	mA	
Soldering Temperature	320	°C	

## **Recommended Operating Conditions**

Parameter	Value	Unit	
Drain Voltage Range	20 - 28	V	
Gate Voltage Range	-5 to -3	V	
Stg 1 Drain Current (Idq)	144	mA	
Stg 2 Drain Current (Idq)	400	mA	

### **Electrical Specifications**

Parameter	Min	Тур	Max	Unit
Operational Frequency	18		23	GHz
Small Signal at 28V				
Small Signal Linear Gain	19	22	23.3	dB
Input Return Loss	-30		-4.2	dB
Output Return Loss	-26		-7.5	dB
	On-Wafer Pulse	d Power at 28V		
Psat (at 25 dBm)	37	38.6	40.3	dBm
Power Gain (at 25 dBm)	12	13.6	15.3	dB
P1db	32.5	33	34.2	dBm
PAE (at 25 dBm)	18	27	35	%
Max PAE	18.8	28.5	35.3	%
Fix	ktured CW at 28\	<mark>/, 25ºC Case Temp</mark>		
Psat (at 25 dBm)	38.4	39.1	39.5	dBm
Power Gain (at 25 dBm)	19.5	21.8	23.3	dB
PAE (at 25 dBm)	22	25.8	30	%
Max PAE	28.7	32	34	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-4.220		V
Stage 2 Gate Voltage		-4.230		V
Stage 1 Idq		144		mA
Stage 2 Idq		400		mA

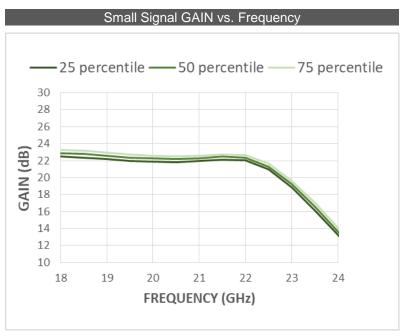
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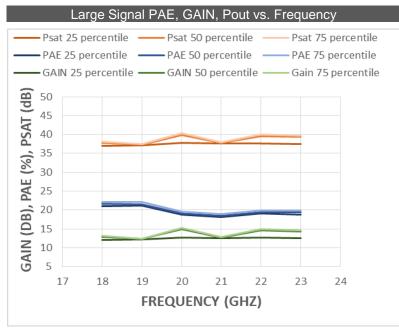
Web: http://www.yeswegan.com

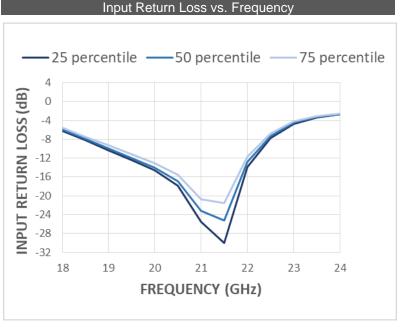


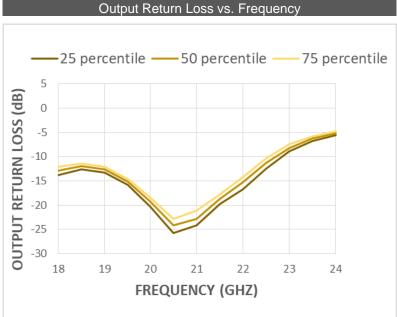
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On wafer measured Performance Characteristics (Typical Performance at 25°C) Vd = 28 V, Id1 = 140 mA, Id2 = 400 mA. \*







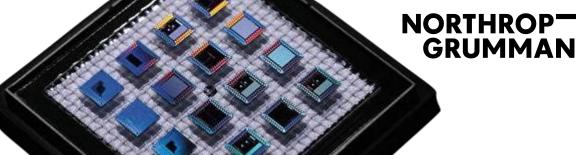


\*Pulsed-power on-wafer

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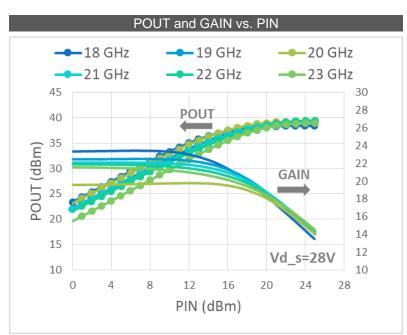
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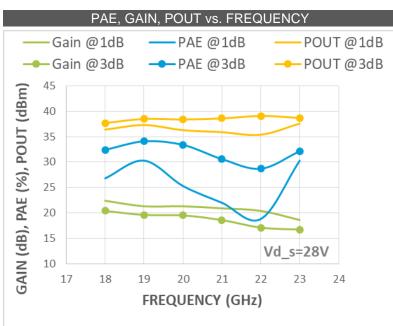
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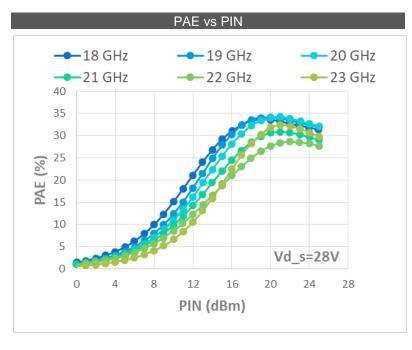


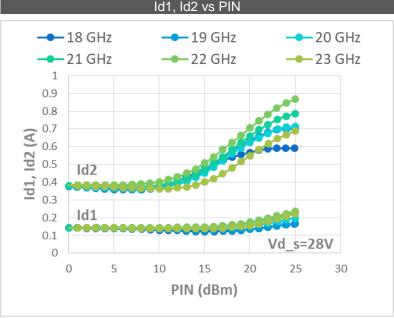
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# Fixture measured Performance Characteristics (Typical Performance at 25°C) Vd = 28.0 V, Id1 = 144 mA, Id2 = 400 mA









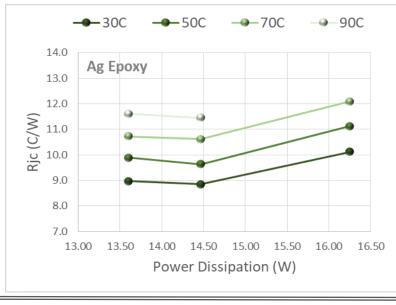
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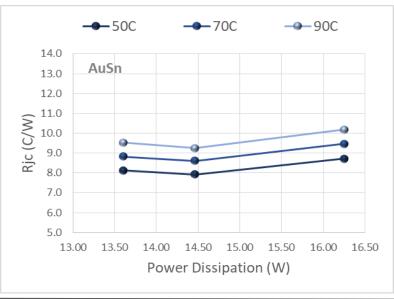
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Preliminary Thermal Properties with die mounted with 25um 80/20 AuSn Eutectic to: 10mil Cu10W Shim.

** \/d = 28 0 \/	1da1 - 1/3 n	nA, Id2q = 375 mA	
$VU = \angle 0.0 V$	1001 = 14311	11A, 10ZQ = 373111A	١

			1 2 2 3 4 1 1 2 1 3 1 3 1 4 2 4 2 1 3 1 3 1 4 1			
Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output	Power Dissipation (W)	Thermal Resistance Rjc (°C/W)
10 mil CuW	AuSn Eutectic	50 °C	161	33.2	13.6	8.1
			164	36.4	14.5	7.9
			192	39.1	16.3	8.7
		70 °C	190	33.2	13.6	8.8
			194	36.4	14.5	8.6
			224	39.1	16.3	9.5
		90 °C	220	33.2	13.6	9.5
			224	36.4	14.5	9.2
			255	39.1	16.3	10.2
10 mil CuW	Ag Epoxy	30 °C	152	33.2	13.6	9
			158	36.4	14.5	8.8
			194	39.1	16.3	10.1
		50 °C	184	33.2	13.6	9.9
			189	36.4	14.5	9.6
			231	39.1	16.3	11.1
		70 °C	216	33.2	13.6	10.7
			223	36.4	14.5	10.6
			266	39.1	16.3	12.1
		90 °C	248	33.2	13.6	11.6
			257	36.4	14.5	11.5





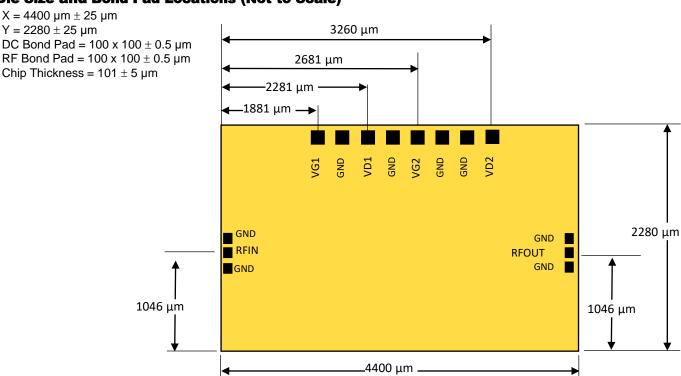
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#### Die Size and Bond Pad Locations (Not to Scale)

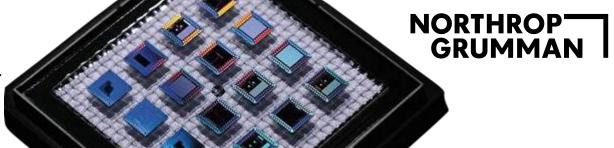


#### **Biasing/De-Biasing Details:**

Bias for 1st stage is from top. The 2nd stages must bias up from both sides.

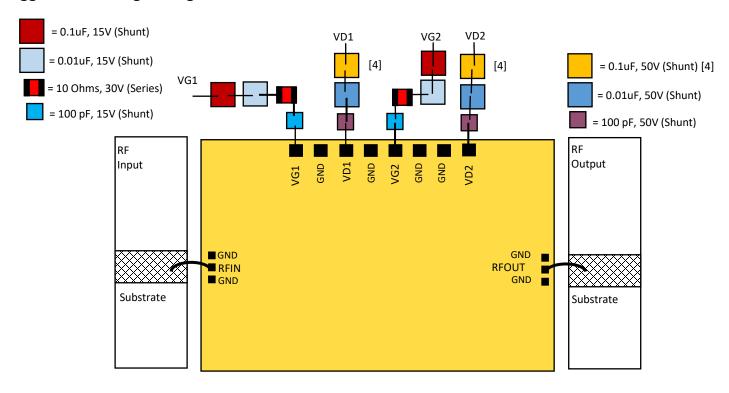
Listed below are some guidelines for GaN device testing and wire bonding:

- a. Limit positive gate bias (G-S or G-D) to < 1V
- b. Know your devices' breakdown voltages
- c. Use a power supply with both voltage and current limit.
- d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
  - i. Apply negative gate voltage (-5 V) to ensure that all devices are off
  - ii. Ramp up drain bias to ~10 V
  - iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
  - iv. Ramp up drain to operating bias
  - v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
- To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
  - i. Gradually decrease drain bias to 0 V.
  - ii. Gradually decrease gate bias to 0 V.
  - iii. Turn off supply voltages
- . Repeat de-bias procedure for each amplifier stage



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#### **Suggested Bonding Arrangement**



#### **Recommended Assembly Notes**

- 1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
- 2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
- 3. Part must be biased from both sides as indicated.
- 4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF, 50V Capacitors.

#### **Mounting Processes**

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

**Note**: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AUSN ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.