**Product Features**
- RF frequency: 80-100 GHz
- Broadband Operation
- Linear gain: 29 dB, typical
- Noise Figure: 2 dB, typical
- P1dB : 3 dBm *
- Microstrip Topology MMIC, In-line Input & Output
- 0.1 um InP HEMT Process
- 3 mil substrate
- DC Power: < 35 mW
- Die Size 1.7 sq. mm

**Performance Characteristics (Ta = 25°C)**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>80</td>
<td>100</td>
<td>100</td>
<td>GHz</td>
</tr>
<tr>
<td>Linear Gain</td>
<td>25</td>
<td>29</td>
<td>29</td>
<td>dB</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>4</td>
<td>10</td>
<td>10</td>
<td>dB</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>5</td>
<td>12</td>
<td>12</td>
<td>dB</td>
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<tr>
<td>Noise Figure</td>
<td>2</td>
<td>3.5</td>
<td>3.5</td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure (Ave.)</td>
<td>2.6</td>
<td>3</td>
<td>3</td>
<td>dB</td>
</tr>
<tr>
<td>P1dB *</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>dBm</td>
</tr>
<tr>
<td>Vd</td>
<td>1.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vg1=Vg2</td>
<td>-0.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Id1</td>
<td>25.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Applications**
- W-Band Imaging
- Sensors
- Radar
- Short Haul / High Capacity Links
- W-Band Communication Links

**Product Description**

The ALP280 W-band InP HEMT Low Noise Amplifier is a 5-Stage, broadband, ultra low noise amplifier MMIC. It can be used in applications such as W-band Imaging, Radar, commercial digital microwave radios and wireless LANs. The small die size allows for extremely compact packaging. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Ti/Au, which is compatible with conventional die attach, thermocompression and thermosonic wire bonding assembly techniques.

**Absolute Maximum Ratings (Ta = 25°C)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd</td>
<td>1.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vg1, Vg2</td>
<td>-1</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Id2</td>
<td>25.5</td>
<td></td>
<td>mA</td>
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<tr>
<td>Input Drive Level *</td>
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<td></td>
<td>dBm</td>
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<tr>
<td>Assy. Temperature</td>
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<td>deg. C</td>
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* Estimated

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Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3 V, Id = 25.5 mA* - Wideband Performance

* On-Wafer, Vg1=Vg2
Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3 V, Id = 25.5 mA* - Performance from 90 GHz to 100 GHz

Linear Gain vs. Frequency

Noise Figure vs. Frequency

Input Return Loss vs. Frequency

Output Return Loss vs. Frequency

* On-Wafer, Vg1=Vg2

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Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3 V, Id = 25.5 mA** - Wideband Performance

* On-Wafer, Vg1 & Vg2 biased Independently
Measured Performance Characteristics (Typical Performance at 25°C)

Vd = 1.3 V, Id = 25.5 mA** - Performance from 90 GHz to 100 GHz

**On-Wafer, Vg1 & Vg2 biased Independently
ALP280
80-100 GHz
Low Noise Amplifier

Die Size and Bond Pad Locations (Not to Scale)

Recommended Assembly Notes
1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of < 6 mil (long) by 1.5 by 0.5 mil ribbons on input and output.
**Suggested Bonding Arrangement**

**Biasing/De-Biasing Details:**

**Bias up sequence:**
- Pinch-off the device by setting \( V_{g1} = V_{g2} = -0.6 \) and \( V_d = 0V \)
- Increase \( V_d \) to the desired value
- Adjust \( V_{g1} = V_{g2} \) to realize the desired \( I_d \) (Nominal Current for \( I_d \) for \( V_{g1} = V_{g2} \) biased on is 25.5 mA)

**Bias down sequence:**
- Reduce \( V_{g1} = V_{g2} \) down to -0.6V
- Lower \( V_d \) to 0V
- Lower \( V_{g1} = V_{g2} \) to 0V

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**Suggested Bonding Arrangement (Alternate Bias)**

Biasing/De-Biasing Details:

**Bias up sequence:**
- Pinch-off the device by setting $V_{g1} = V_{g2} = -0.6$ and $V_d = 0V$
- Increase $V_d$ to the desired value
- Adjust $V_{g1}$ to realize the desired $I_d$ (Nominal Current for $I_d$ for $V_{g1}$ biased on is 13.5 mA)
- Adjust $V_{g2}$ to realize the desired $I_d$ (Nominal Current for $I_d$ for both $V_{g1}$ and $V_{g2}$ biased on is 25.5 mA)

**Bias down sequence:**
- Reduce $V_{g2}$ down to -0.6V
- Reduce $V_{g1}$ down to -0.6V
- Lower $V_d$ to 0V
- Lower $V_{g1}$ and $V_{g2}$ to 0V

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