Product Features

- RF frequency: 16 to 20.8 GHz
- Linear Gain: 10 dB typ.
- Psat: 39 dBm typ.
- Efficiency @ P3dB > 40%
- Die size = 9 sq. Mm
- 0.2um GaN HEMT
- 4 mil SiC substrate
- DC Power: 20 VDC @ 256 mA

Product Description

The APN293 monolithic GaN HEMT amplifier is a broadband, one-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, and Radar Applications. To support rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Applications

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

Performance Characteristics (Ta = 25°C)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>16</td>
<td></td>
<td>20.8</td>
<td>GHz</td>
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<tr>
<td>Linear Gain</td>
<td>9</td>
<td>10</td>
<td></td>
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<tr>
<td>Input Return Loss</td>
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<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Return Loss</td>
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<td>17</td>
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<td>dB</td>
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<tr>
<td>P1db</td>
<td>36</td>
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<td>dBm</td>
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<tr>
<td>Psat</td>
<td>37.5</td>
<td>38.5</td>
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<td>dBm</td>
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<tr>
<td>PAE @ Psat</td>
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<td>%</td>
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<tr>
<td>Vd1, Vd2</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vg1</td>
<td>-3.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vg2</td>
<td>-3.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Id1</td>
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<td></td>
<td>mA</td>
</tr>
<tr>
<td>Id2</td>
<td>400</td>
<td></td>
<td></td>
<td>mA</td>
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Maximum SOA Ratings (Ta = 25°C)

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<tr>
<th>Parameter</th>
<th>Min</th>
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<tr>
<td>DC Power</td>
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<td>W/mm</td>
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<tr>
<td>Vd1, Vd2</td>
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<td>28</td>
<td>V</td>
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<tr>
<td>Id1</td>
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<td></td>
<td>mA</td>
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<tr>
<td>Id2+ld2a</td>
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<td></td>
<td>mA</td>
</tr>
<tr>
<td>Vg1, Vg2</td>
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<td>V</td>
</tr>
<tr>
<td>Assy. Temperature</td>
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<td>deg. C</td>
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</table>
APN293
16-20.8 GHz
GaN Power Amplifier

Advance Datasheet
Revision: April 2019

Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 20.0 V, Id1 = 144 mA, Id2 = 400 mA *

Linear Gain vs. Frequency

Power, Gain, PAE% vs. Frequency

Return Loss vs. Frequency

* Pulsed-Power On-Wafer

Preliminary Information: The data contained in this document describes new products in the sampling or preproduction phase of development and is for information only. Northrop Grumman reserves the right to change without notice the characteristic data and other specifications as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained in the Export Administration Regulations (EAR). Export out of the U.S. may require a U.S. Bureau of Industry and Security export license.

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**Die Size and Bond Pad Locations (Not to Scale)**

- X = 3000 µm ± 25 µm
- Y = 3000 ± 25 µm
- DC Bond Pad = 100 x 100 ± 0.5 µm
- RF Bond Pad = 100 x 100 ± 0.5 µm
- Chip Thickness = 101 ± 5 µm

**Biasing/De-Biasing Details:**

Bias is single sided and is from the top only.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices’ breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
   i. Apply negative gate voltage (-5 V) to ensure that all devices are off
   ii. Ramp up drain bias to ~10 V
   iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
   iv. Ramp up drain to operating bias
   v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
   i. Gradually decrease drain bias to 0 V.
   ii. Gradually decrease gate bias to 0 V.
   iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage
Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do NOT use the 0.1uF, 50V Capacitors.

Mounting Processes

Most NGSC GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSC recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGSC parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO NGSC “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS.