



## **GaN IC Die Handling, Assembly and Testing Techniques**

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## **1. Scope**

This document describes the storage and handling requirements for GaN IC chips. It also describes recommended assembly and testing techniques for users of GaN IC chips. Chips are usually delivered to the end user as individual chips stored in plastic chip trays or Gel-Pak. This document provides guidelines to aid the user in the assembly of GaN IC die in a manner consistent with desired electrical performance.

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### **1.1 Organization of Document**

This document addresses the following areas:

- Packaging for shipment: Paragraph 3.1
- Allowable storage conditions: Paragraph 3.2
- Recommended assembly processes: Paragraph 3.3
- External Components: Paragraph 3.4
- Electrostatic discharge sensitivity (ESD): Paragraph 3.5
- General Testing Guidelines: Paragraph 3.6

## **2. Applicable Documents**

The “MIL\_STD\_883, Test Methods and Procedures for Microelectronics” is referenced in this document.

## **3. Handling Requirements and Process Recommendations**

### **3.1 Packaging for Shipment**

GaN chips may be as thin as 4 mils (100 microns) at their thickest point. Due to this, it is necessary to treat GaN chips with care. Chips are packaged in Fluoroware (or equivalent) anti-static chip trays or Gel-Pak boxes. The container is wrapped in a shock absorbent material, such as bubble-pack prior to boxing the shipment.



## 3.2 Allowable Storage Conditions

Compared to many other microelectronic devices, GaN chips are relatively durable under a wide range of storage environments. NGAS's GaN ICs have no exposed materials that can easily corrode or degrade. All exposed metallizations are gold, and all active devices are passivated with silicon nitride. It is obviously essential that the storage environment be free of any substance that can degrade these materials. Long-term exposure to concentrated agents capable of corroding SiC or other metals is also not recommended, since the passivation layers are thin and not completely impervious.

### 3.2.1 Recommended Atmosphere

Although not necessary, a clean, dry nitrogen atmosphere is recommended for storage. Normal ambient air will not damage GaN devices, but if the chips are allowed to become wet or dirty, they will be difficult to clean.

### 3.2.2 Storage Temperatures

NGAS's GaN ICs are recommended to be stored at room temperature (25 ± 3C). NGAS's GaN ICs can be stored at 125 C indefinitely without damage. GaN chips are capable of surviving much higher temperatures for shorter times.

## 3.3 Recommended Assembly Process

### 3.3.1 Individual Chip Handling

The metallization patterns on the frontside of the chip are very fragile. Any tool that contacts the frontside of the chip must be used with extreme caution. Vacuum pickup tools may be used on GaN chips, but NGAS recommends that the proper tool be used that minimizes contact with sensitive elements of the chip. Vacuum pickup tools that contact the backside of the chip, center of the chip, or edges of the chip should be selected to minimize contact to sensitive areas of the chip. Sensitive areas include airbridges, transistors, diodes, capacitors, and thin film resistors. If tweezers are used, it is recommended to use ESD compliant tweezers.

**Note:** Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.



### 3.3.2 Personnel Training

Assembly operators familiar only with silicon ICs or ceramic substrates should be retrained specifically for handling GaN chips. NGAS has learned that many people hired without previous GaN experience require a period of training and practice before they can safely and confidently handle GaN chips.

### 3.3.3 Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320oC for 30 seconds.

**Note:** Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

**CAUTION:** THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

### 3.3.4 Grounding

The back of the chip is the ground plane so it is imperative that it sees a good ground connection. Without good grounding the chip could see an increased inductance and/or resistance to ground. The result of this is the potential for oscillations.

The Ground pads on the top of the chips are for wafer probing only. They do not require being bonded. The On chip Ground pad SHOULD NOT be used as an alternative to providing the back plane with an adequate ground.

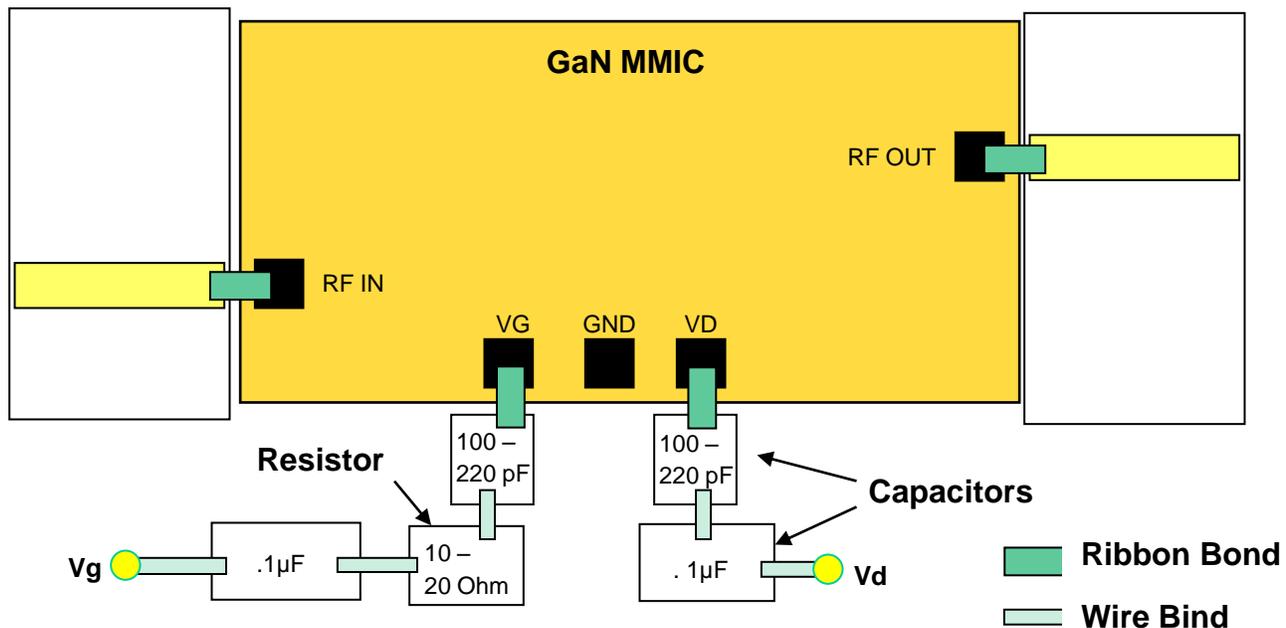
**3.3.5 Ribbon/Wire Bonding**

Figure 1 shows a typical GaN IC chip bonding approach.

NGAS GaN IC chips have gold metallization on all bond/probe pads and are therefore suitable for both gold wire and ribbon bonding. When a proper bonding schedule is used, the bond strength and pad adhesion are capable of meeting the destructive bond pull limits in MIL\_STD\_883.

To attach the RFIN / RFOUT pads to the substrate either a ribbon or a wire can be used. The lengths should be kept to a minimum to limit the inductance and possible affect it can have on the performance of the chip. The preferred method is to use a wedge bond.

The first Ribbon/Wire in the bias line (from the chip to the 100 - 220pF single layer capacitor) is the most critical. If a long wire is used, it could form a resonant circuit with the 100 - 220pF capacitor and cause an oscillation.



**Figure 1: Representative GaN HEMT Bonding**

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**3.3.5 Ribbon/Wire Bonding (cont.)**

**General recommendations for wire/ribbon bonding are:**

- a. Ball bonding is not recommended for signal path bonds due to potential ESD issues.
- b. The safest, most reliable technique utilized at NGAS, is a thermosonic wedge bonder.
- c. Provide proper grounding for the bonder equipment and all peripheral equipment, including heated stages and wire feeds.
- d. Ensure that the bonders are grounded and are free of any transients.
- e. The tooling recommendations for gold wire and gold ribbon are listed in Table I.
- f. It is critical in GaN assembly to establish a proper bond schedule; too little power applied will result in a weak bond. On the other hand, too much power may damage the pad and even delaminate the pad from the substrate. Please check the guidelines for your specific machine.
- g. Ground substrate bonding pads, traces and capacitors before bonding to sensitive devices. Remove these wires before electrical testing.
- h. Use an oscilloscope to ensure the absence of dynamic voltage transients at the bonding tip of wire bonding equipment with the probe connected to the bond head, and the probe ground connected to the stage. Use a multimeter to check the resistance from the bonding tip and stage of the wire bonder to ground. Ensure that all bonding equipment which comes into contact with the device/IC is grounded. Perform regular periodic checks of all equipment as part of a preventative-maintenance program. .
- i. Bond to grounded bond pads before bonding to device bond pads. Bond to DC bond pads before RF bond pads. Back bonding effectively provides a ground path for any voltage on the bonding tip.

**Table I. Gold Wire/Ribbon Description and Tooling**

	<b>Gold Wire</b>	<b>Gold Ribbon</b>
Use	• Low frequency signal paths	• RF signal paths • Capacitors to MMIC
Size	1 mil diameter	3 x 0.5 mil

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### 3.4 External Components

These are the recommended off chip bias components to insure that the electrical performance of the chip matches the performance as seen in the data sheets.

#### 3.4.1 Capacitors

##### 1. 100 - 200pF Cap

The first bias bypass capacitor should be a 100 – 220pF ceramic (single layer) capacitor, placed no farther than 30 mils from the MMIC and connected to the MIMIC by ribbon bond.

##### 2. 0.1uF

The second bias bypass capacitor helps to eliminate any other very low frequency problems.

\*Note: If you are tying multiple gates/drains together, the best place to tie them together is at the 0.1uF capacitor. This will help to prevent instability

#### 3.4.2 Resistors

##### 1. 10 – 20 Ohm Resistor

The 10 - 20 Ohm resistor on the gate line is used to de-Q the bias path to minimize the potential for oscillations.

### 3.5 Electrostatic Discharge Sensitivity

Electrostatic discharge(ESD) refers to excessive voltage applied to a chip, generally as a result of contact with an ungrounded human body. ESD damage thresholds measured on NGAS GaN devices per MIL-STD-883, Method 3015 (Human Body Model) are listed in Table II. The data in Table II is measured with the ESD applied to the gate and with the source grounded. This represents the worst-case, or most sensitive circuit topology. At NGAS all GaN IC products are treated and handled as ESD sensitive Class 0, both during and after the time the individual chips are diced out of the wafer. The risk of ESD damage to the chips while they are still in wafer form is actually small, except during probe testing. During probe testing, electrostatic discharges could be applied to the sensitive device terminals through the probes.

Recommended procedures for preventing ESD damage are listed below:

- Adequately train personnel in the prevention of ESD damage before they handle GaN devices.
- Follow ESD prevention procedures throughout assembly and test. Use pin-to-case grounding, or pin shielding, or back bonding (see paragraph 3.3.4) whenever possible.
- Store GaN chips and wafers in anti-static containers. For chip trays, also known as waffle packs), NGAS recommends Fluoroware STAT-PRO 400 trays.
- Ensure that all equipment is properly grounded and isolated from each other.
- Handle GaN chips only at workstations properly equipped with ESD-prevention products and materials (e.g. grounded wrist straps, grounded table tops, etc.)

**Table II. G-S damage threshold from Electrostatic Discharge**

**(MIL-STD-883, Method 3015)**

Device	Damage Threshold Positive Polarity (V)	Damage Threshold Negative Polarity (V)
GaN 0.25/0.20 um Power-HEMT (device)	10*	> 80

\* Failed at first 10V step.

### 3.6 General testing guidelines

Listed below are some guidelines for GaN device testing and wire bonding:

- a. Limit positive gate bias (G-S or G-D) to < 1V
- b. Know your devices' breakdown voltages
- c. Use a power supply with both voltage and current limit.
- d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
  - i. Apply negative gate voltage (-5 V) to ensure that all devices are off
  - ii. Ramp up drain bias to ~10 V
  - iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
  - iv. Ramp up drain to operating bias
  - v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
- e. To safely debias GaN devices, start by debiasing output amplifier stages first (if applicable):
  - i. Gradually decrease drain bias to 0 V.
  - ii. Gradually decrease gate bias to 0 V.
  - iii. Turn off supply voltages
- f. Repeat debias procedure for each amplifier stage

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**Table III. Summary of NGAS's GaN IC Handling Recommendations**

	<b>Recommended Practice</b>	<b>Comments</b>
<b>Packaging Chips</b>	Store in individual chip trays (Fluoroware, STAT-PRO 400, or equivalent).	
<b>Storage General</b>	Avoid exposure to corrosive materials.	Exposed surfaces (gold and silicon nitride) are corrosion resistant, but still require careful handling.
<b>Atmosphere</b>	Store in dry nitrogen.	Normal air is not damaging, but care must be taken to avoid chips becoming wet or dirty.
<b>Temperature</b>	Store below 125C.	Chips can withstand higher temperatures for short periods of time.
<b>Assembly Chip Handling</b>	Use extreme caution with tools that contact the frontside of the chip.	Verify that any vacuum pick-up tool which contact the front of the chip do not cause damage, or only use tools against the backside of the chip.
<b>Training</b>	Personnel require training and practice to safely handle GaN chips.	Previous experiences with silicon IC chips or ceramic substrates does not qualify for GaN chips.
<b>Mounting</b>	Mount with conductive epoxy.	NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320oC for 30 seconds
<b>Wire Bonding</b>	Manual, wedge-wedge gold ribbon bond tool, with no flame-off feature. Employ back bonding where possible. Always check the voltage on the bonding tip with an oscilloscope before bonding.	Ball bonding is not recommended. Wire bonding equipment can generate dangerous voltages at the tip or stage. Monitor all bonding equipment regularly.
<b>Electrostatic Discharge Protection</b>	Follow recommendation in Paragraph 3.5	Treat all GaN IC chips as Class 0 ESD sensitive.

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