

Laser Diode Fabrication Capabilities at CEO

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ABSTRACT

Northrop Grumman's subsidiary, Cutting Edge Optronics (CEO) has been processing and facet coating high-power laser diode wafers and edge-emitting quantum well laser diodes for over 20 years. These laser diodes range across the near-infrared spectrum from 640nm to 1650nm and provide output powers from tens to hundreds of watts per device. These designs are based both on internal epitaxial designs as well as customer designed structures.

INTRODUCTION

CEO is a vertically integrated manufacturer of diode lasers. We fabricate full commercial, industrial and military laser systems as well as the components that make up these systems such as the laser diodes, diode arrays, gain modules and control electronics. These components, beginning with processed epitaxial wafers, are not only used in our own products but also sold directly to original equipment manufacturers (OEM). Our vertically integrated manufacturing facility is ISO 9001-2015 certified. Epitaxial wafer processing is completed in class 100 clean rooms. Diodes are fabricated, characterized and assembled in class 1,000 to 10,000 clean rooms. All research and development (including epitaxial design), manufacturing and testing is completed in this facility.

The fundamental building block of these systems is the high power semiconductor quantum-well laser diode. These devices are used in a wide variety of medical, automotive, military, industrial, and scientific applications. They are valuable because of their ability to efficiently generate coherent light output in a narrow wavelength band. Because of this they can be used as efficient pump sources for solid-state lasers. Alternatively, they can be used as direct light sources for a wide range of applications such as welding, ablation, and covert illumination.

CEO has experience processing and coating laser diodes with operational wavelengths ranging from 630nm to 1650nm. Epitaxial structures are grown onto purchased semiconductor wafers (e.g. GaAs, InP, InGaP, etc.) by qualified suppliers. Wafer processing, die fabrication and optical coating is completed at CEO. The process flow used to fabricate these devices is shown in Figure 1. This paper provides a more detailed look at each of these capabilities.

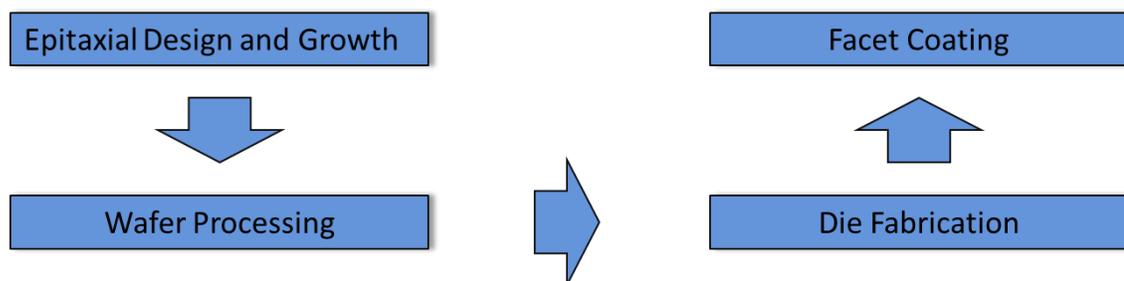


Figure 1. Process flow for the fabrication of high power laser diode devices.

PHOTOMASK DESIGN

All of the photomasks used to process wafers at CEO are designed and laid out in-house. The mask layout data files are then sent to an external vendor for fabrication. CEO's in-house layout capability enables a very short lead time of as little as two weeks between wafer design concept and in-hand photomasks.

WAFER PROCESSING

Many of the critical features of a laser diode are created during wafer processing. Figure 2 shows an example cross section of an edge-emitting quantum-well laser. Photolithography is used to pattern all of the critical features shown in in fixture 1, including the mesas, V-grooves, and insulator openings (contacts). This process consists of coating the wafer with a photosensitive film (photoresist), patterning the photoresist by exposing defined areas to the resist to UV light using a photomask, developing the resist pattern, then etching the final pattern into the wafer. Plasma enhanced chemical vapor deposition (PECVD) of silicon oxide or nitride may be used to create the insulator layer. The V-grooves, mesas, and contact openings can be created by wet chemical etching and reactive ion dry/plasma etching is used to create the features of the insulator layer. Sputter deposition is then used to add a p-side contact metals stack, typically consisting of a titanium-tungsten adhesion layer, a platinum barrier layer, and a gold top layer. These metals create an ohmic contact on the diode and also provide a good interface for soldering and wire-bonding.

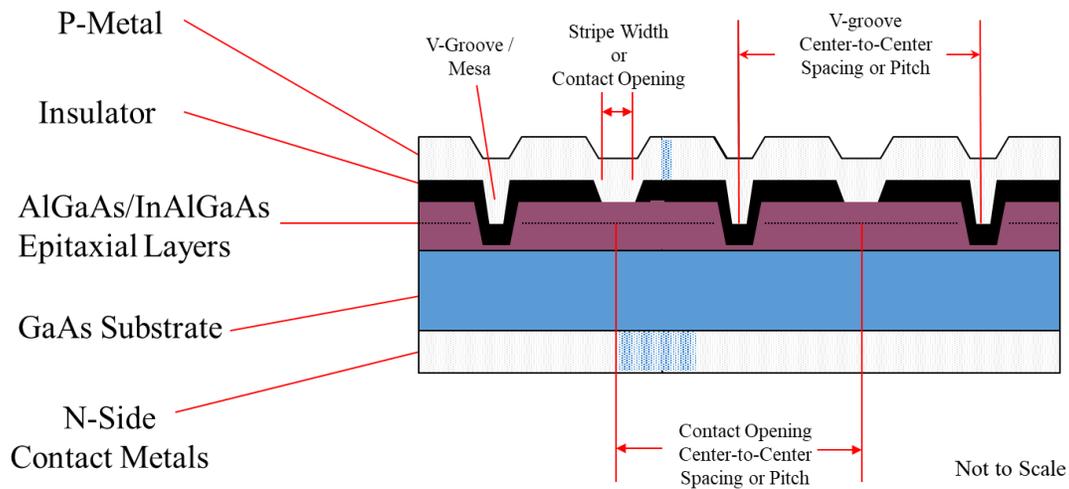


Figure 2. Example cross section of a laser diode device.



Figure 3. Wafer Processing is completed inside of a class 100 clean room at CEO.

The above process steps are all completed on an epitaxial wafer which typically has a thickness of approximately 625 microns. It is -desirable for the final device thickness to be considerably less than this. Minimizing the thickness of the device allows electrical series and thermal resistances to be reduced and also allows devices to be vertically stacked with reduced device to device spacing, or 'pitch'. The wafers are thinned to the desired device thickness by lapping and chemical-mechanical polishing (CMP). The wafer is first mechanically lapped using an abrasive water and ceramic slurry. The lapping process results in microscopic damage to the surface. This damage is then removed and the wafer is thinned to its final thickness by chemical mechanical polishing. The wafer is typically thinned to a final thickness (typically 100-200 microns) during the lap and polish process. The n-side is then metallized by sputtering layers of gold, germanium, and nickel on the n-side, then completing a rapid, high-temperature thermal cycle to intermix, or alloy, these layers with the semiconductor, resulting in an ohmic contact with very low contact resistivity. Additional metal layers may be sputtered or plated over the n-side ohmic contact as necessary to provide a suitable interface for soldering or wire bonding.

DIE FABRICATION

Fabrication of individual laser diode bars follows the completion of wafer processing. Tens to hundreds of individual diode bars are produced from a single processed wafer during this set of processes. The first step is the scribing columns which will be used to cleave the wafer into individual laser diode bars. The wafer is placed onto a thin film. Semi-automated scribe and cleave systems use a diamond tipped tool to create damage sites (scribe) at the desired break locations. The column width matches the desired bar width and is usually approximately 1 cm wide. The bar pattern is carefully aligned during wafer processing such that the columns are formed along the crystalline planes of the wafer. Once the scribe marks are made on the wafer a bending force is applied to propagate the desired break along the crystalline plane of the wafer. The individual columns can now be cleaved into rows in the same manner. The dimension of the rows is defined by the cavity length of a given bar design. The cavity length typically ranges from 0.625 millimeters to 4 millimeters. Therefore a 3" processed wafer will typically yield from 100 to over 400 bars and 175 to 700 bars can be yielded from a 4" wafer.



Figure 4. A wafer is shown cleaved into columns. This wafer will later be cleaved into rows forming individual diode bars.

FACET COATING

The next step of the die fabrication process is the coating of the cleaved facets. CEO has the capability of designing and depositing a wide range of dielectric facet coatings. Typically a $\frac{1}{4}$ wave coating of dielectric materials (such as SiO_2 , Al_2O_3 , MgF , TiO_2 , HfO_2 , or Ta_2O_5) is used to form a low anti-reflectivity (AR) coating of approximately 3-8% on the output surface. Custom AR coatings such as non-quarter wave designs targeting a specific reflectance, or very low reflectivity coatings of <1% are also possible for applications that may benefit from them such as the use of an external cavity. The facet opposite of the output facet typically receives a high reflectivity (HR) coating of approximately 99%. This coating is formed by depositing alternating layers of high- and low-refractive index dielectric materials.

CEO has invested a considerable amount of capital funds recently into the facet coating processes. This includes new laser diode facet coaters as well as laser diode bar and chip handling equipment. All critical die fabrication processes are completed in class 100 cleanrooms which minimize particle-induced defects and improves overall reliability. Semi-automated bar loading stations are used to stack the cleaved laser diode bars into fixtures. The stacked bars are clamped in the fixture with their cleaved edges exposed for the subsequent facet coating process. The facet surfaces may be cleaned under vacuum. Alternatively a thin passivation layer can be deposited underneath the AR/HR high-density coatings. The facet coatings can be deposited through either electron beam thermal evaporation or Ion Beam Sputtering (IBS). Once both the AR and HR coatings are complete the bars are unloaded using the bar loading stations. Each laser diode bar is then optically inspected to insure that both facets as well as the p-side surface meet all requirements.

CONCLUSION

Cutting Edge Optronics has over 20 years of experience fabricating high power laser diode bars. This includes full wafer processing and scribe, cleave and coat capabilities. All research and development (including epitaxial design), manufacturing and testing is completed in CEO's U.S. facility. The critical die fabrication processes are completed in class 100 cleanrooms. The fabricated laser diodes are integrated into diode arrays, laser amplifier modules and fully laser systems and are also sold directly to OEM's for integration into their laser products.