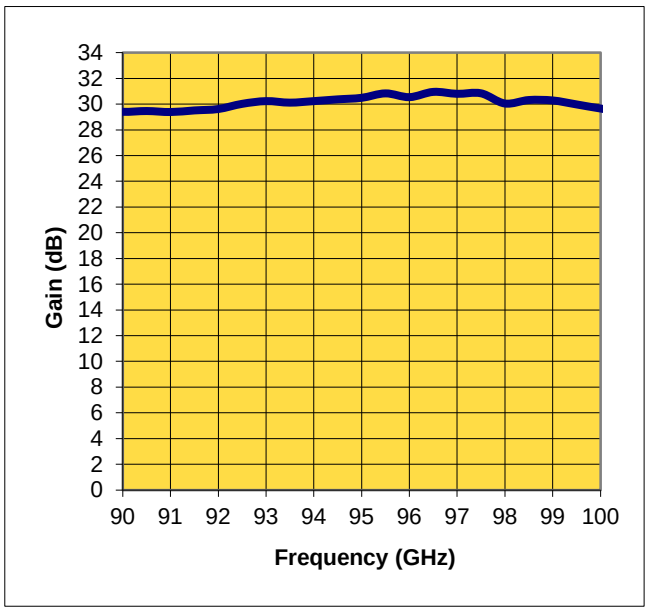
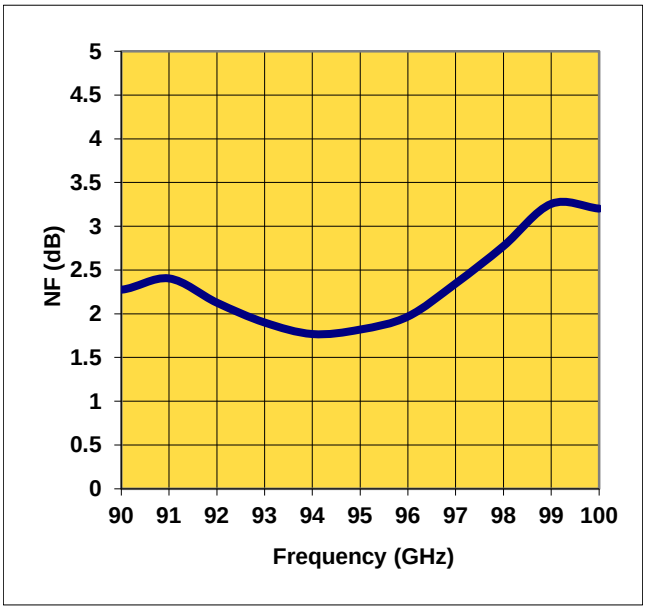
Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3 V, Id = 25.5 mA* - Performance from 90 GHz to 100 GHz

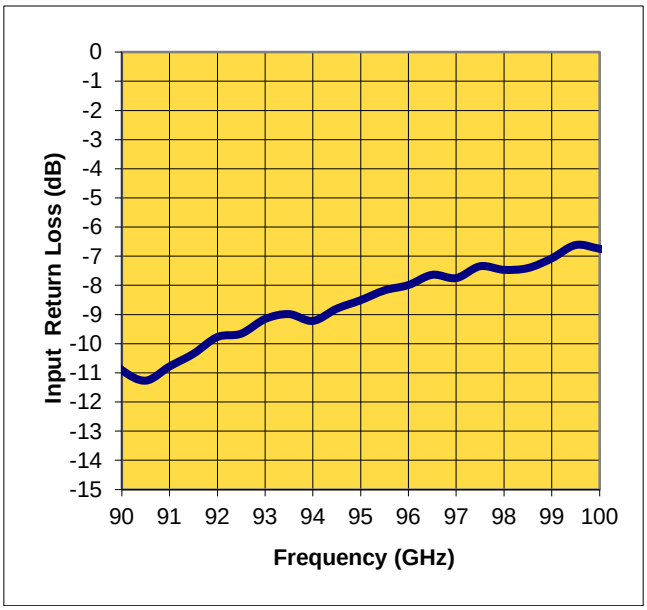
Linear Gain vs. Frequency



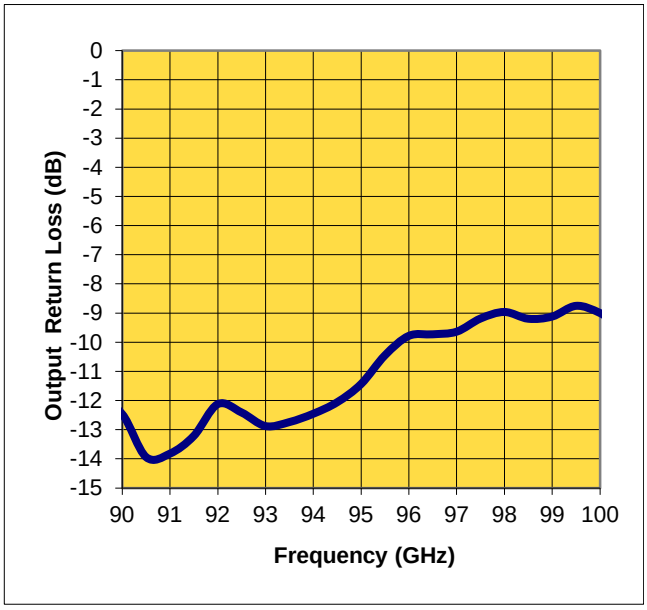
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer, Vg1=Vg2

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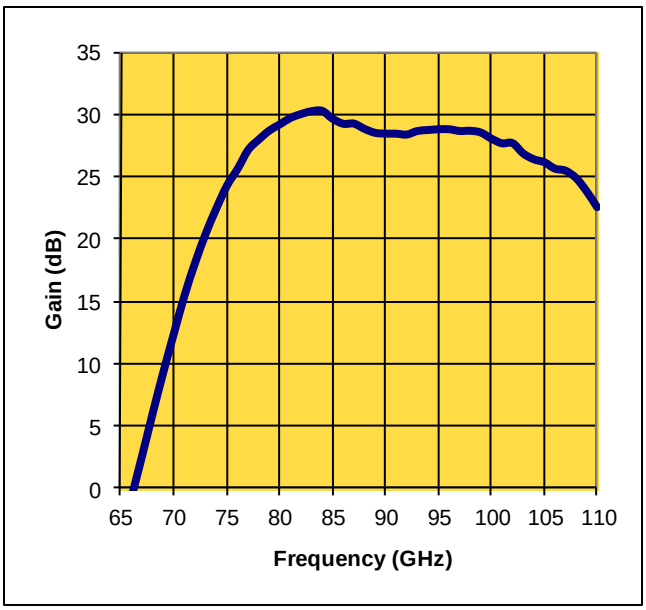
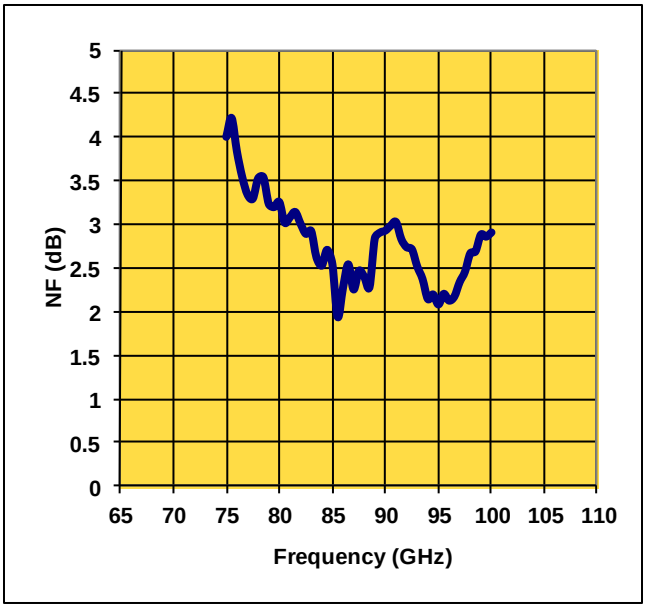
Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3 V, Id = 25.5 mA** - Wideband Performance

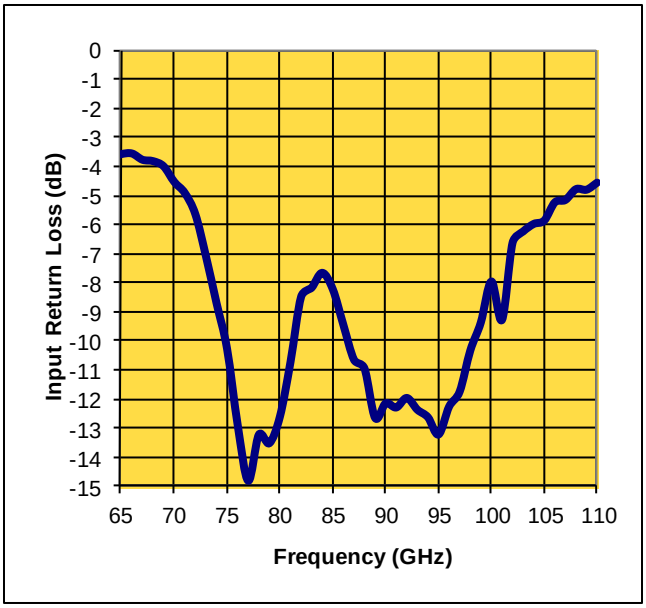
Linear Gain vs. Frequency



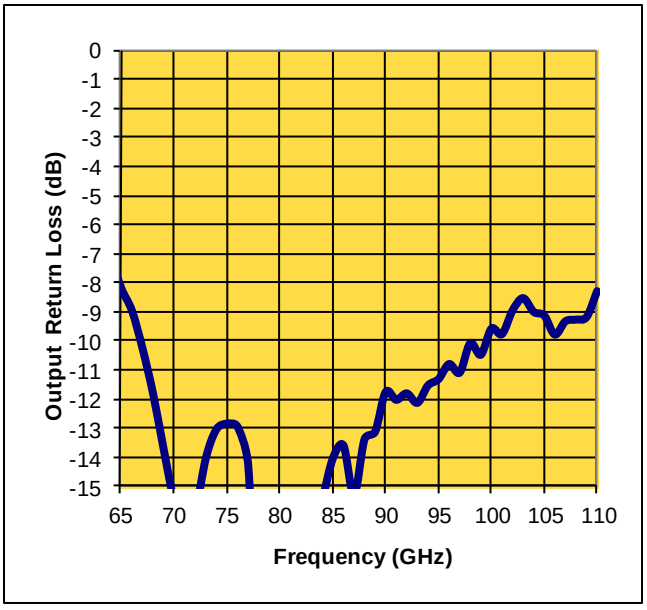
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer, Vg1 & Vg2 biased Independently

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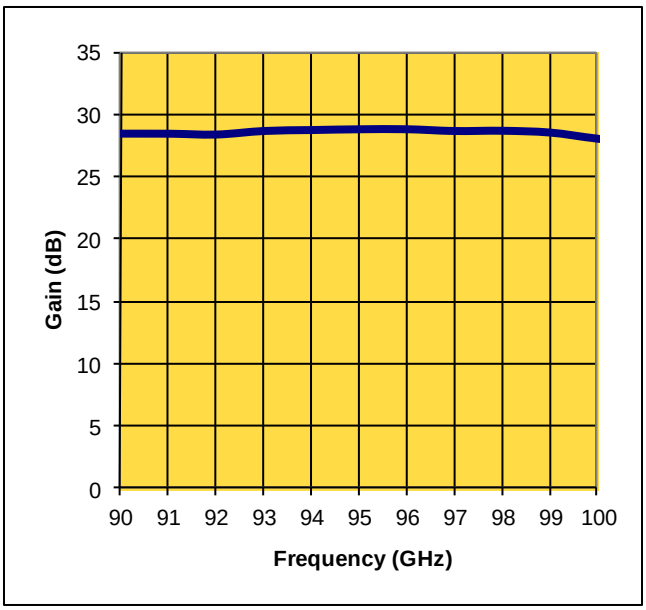
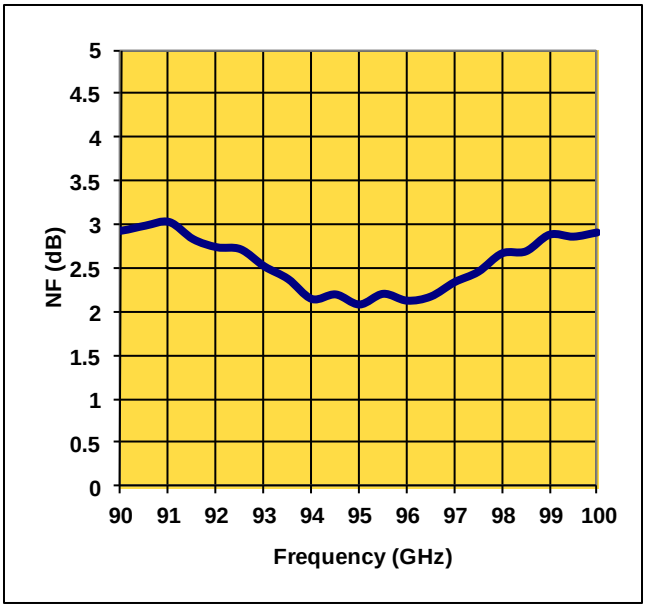
Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3 V, Id = 25.5 mA** - Performance from 90 GHz to 100 GHz

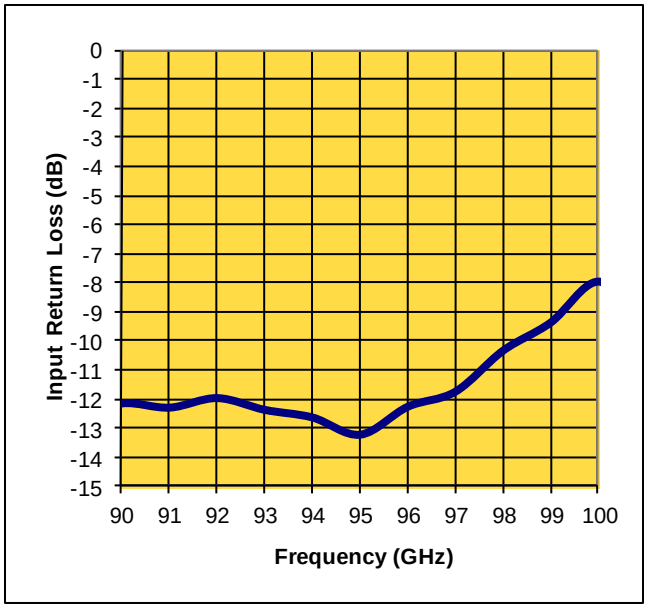
Linear Gain vs. Frequency



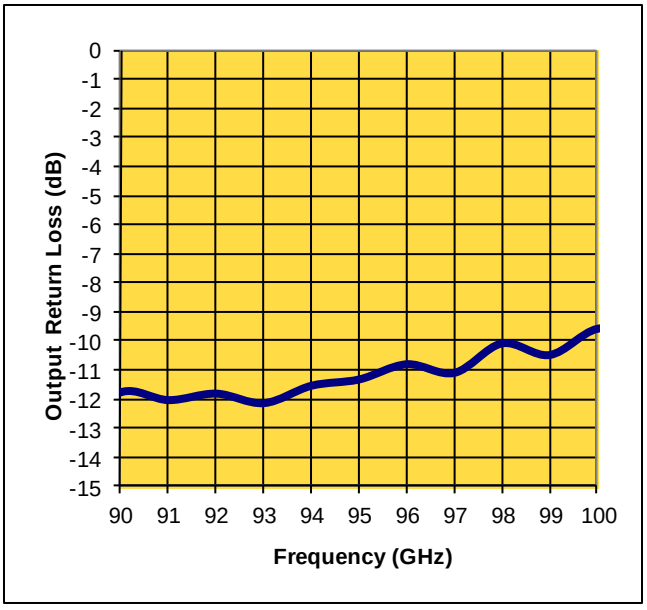
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



* On-Wafer, Vg1 & Vg2 biased Independently

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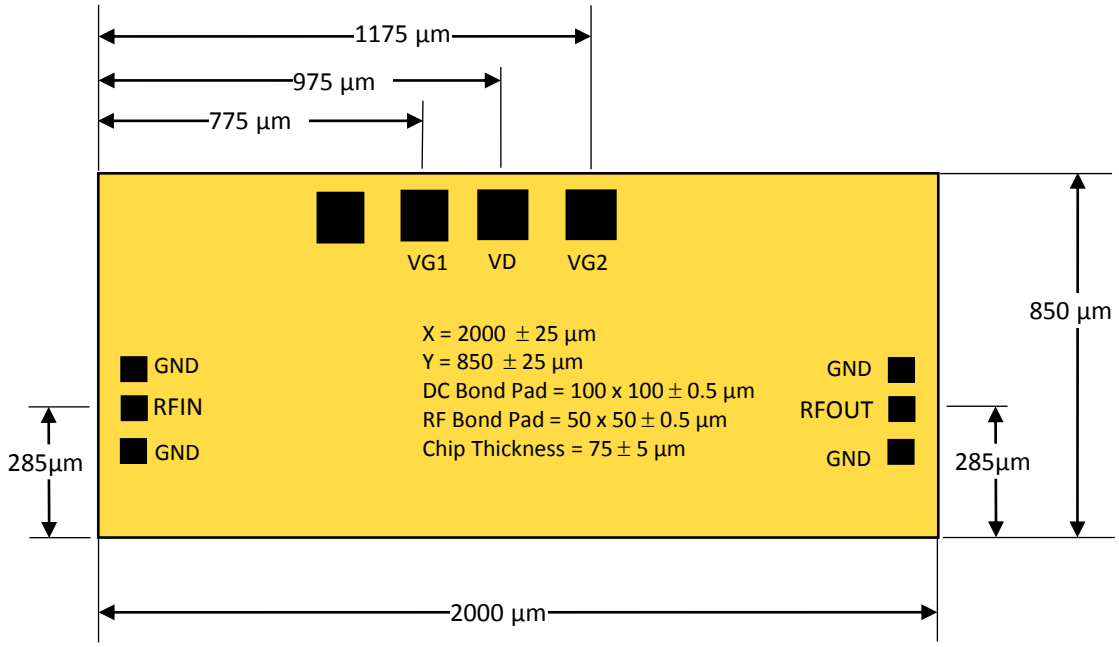
Die Size and Bond Pad Locations (Not to Scale)



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of < 6 mil (long) by 1.5 by 0.5 mil ribbons on input and output.

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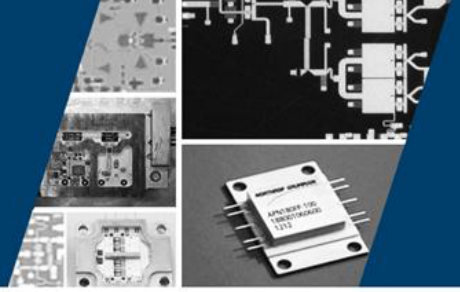
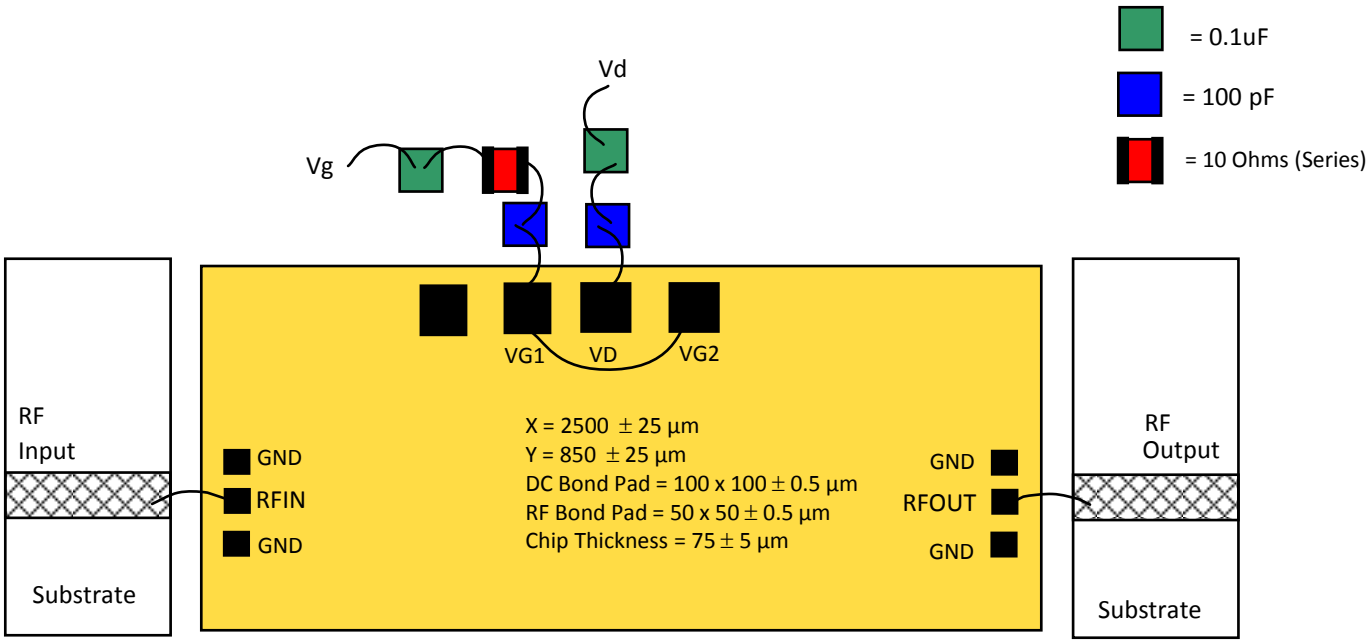


Suggested Bonding Arrangement



Biasing/De-Biasing Details:

Bias up sequence:

Pinch-off the device by setting Vg1 = Vg2= -0.6 and Vd = 0V
Increase Vd to the desired value
Adjust Vg1=Vg2 to realize the desired Id (Nominal Current for Id for Vg1 = Vg2 biased on is 25.5 mA)

Bias down sequence:

Reduce Vg1=Vg2 down to -0.6V
Lower Vd to 0V
Lower Vg1=Vg2 to 0V

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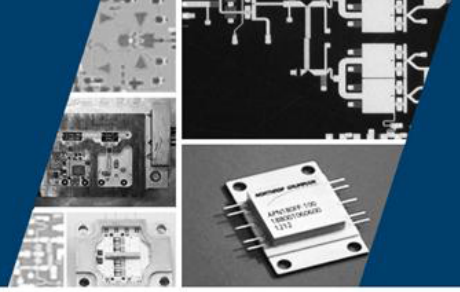
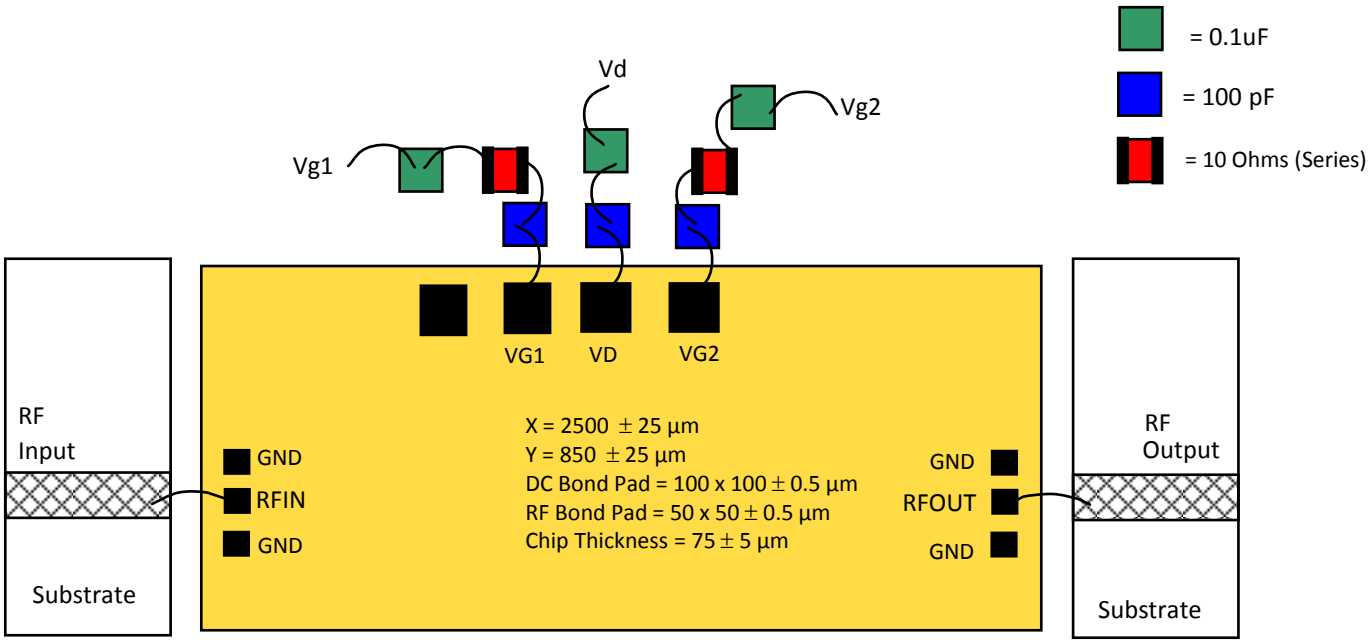


Suggested Bonding Arrangement (Alternate Bias)



Biasing/De-Biasing Details:

Bias up sequence:

Pinch-off the device by setting Vg1 = Vg2= -0.6 and Vd = 0V
Increase Vd to the desired value
Adjust Vg1 to realize the desired Id (Nominal Current for Id for Vg1 biased on is 13.5 mA)
Adjust Vg2 to realize the desired Id (Nominal Current for Id for both Vg1 and Vg2 biased on is 25.5 mA)

Bias down sequence:

Reduce Vg2 down to -0.6V
Reduce Vg1 down to -0.6V
Lower Vd to 0V
Lower Vg1 and Vg2 to 0V

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