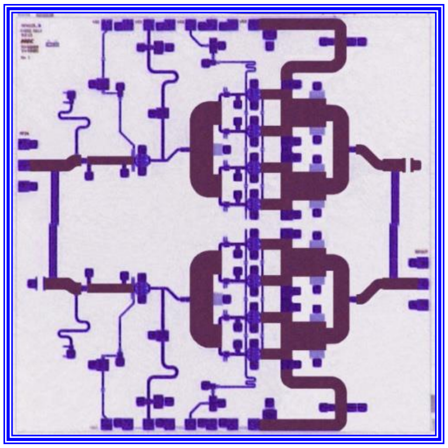
APN228
27 – 31 GHz
GaN Power Amp

NORTHROP GRUMMAN

Revision 2022-1



x=4.0 mm; y=4.0 mm

Product Description

The APN228 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in SatCom Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

Product Features

- RF frequency: 27 to 31 GHz
- Linear Gain: 16 dB typ.
- Psat: ~16 W on wafer, typical
- Psat: ~12.5 W (CW)
- Die Size: 16 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 1.2 A

Export Information
ECCN: **3A001.b.2.c**
HTS (Schedule B) code: **8542.33.0001**

* Pulsed-Power On-Wafer unless otherwise noted

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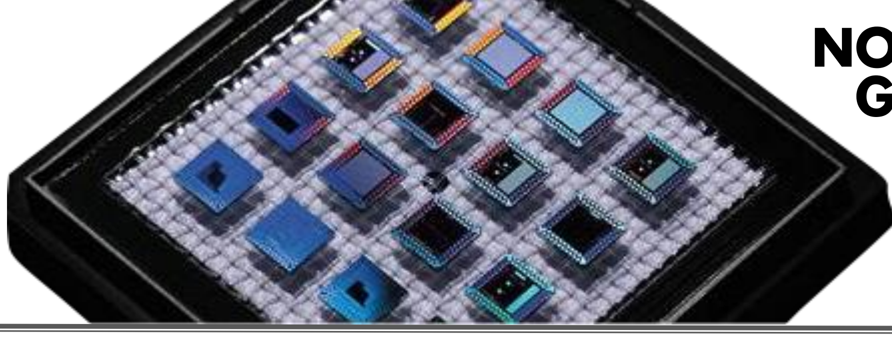

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Absolute Maximum Ratings

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	1500	mA
Gate Current	0.6	mA
Power Dissipation*	42	W
Soldering Temperature	320	ºC

*7W/mm of gate periphery

Recommended Operating Conditions

Parameter	Value	Unit
Drain Voltage Range	20 - 28	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	240	mA
Stg 2 Drain Current (Idq)	240 – 960	mA

Electrical Specifications

Parameter	Min	Typ	Max	Unit
Operational Frequency	27		31	GHz
Small Signal at 28V				
Small Signal Linear Gain	18.5		20	dB
Input Return Loss	-35		-20	dB
Output Return Loss	-26		-16	dB
On-Wafer Pulsed Power at 28V				
Psat (at 27 dBm)		42		dBm
Power Gain (at 27 dBm)	19.1	19.6	20.1	dB
P1db	41.20	42	42.5	dBm
PAE (at 27 dBm)	30.5	32.5	34	%
Max PAE	31	32.9	33.8	%
Fixtured CW at 24V, 25ºC Case Temp				
Psat (at 28 dBm)	38.1	39	39.6	dBm
Power Gain (at 28 dBm)	15.3	16.9	17.8	dB
PAE (at 28 dBm)	19.1	22	24.7	%
Max PAE	24		28.4	%
Drain Voltage		28		V
Stage 1 Gate Voltage		-3.925		V
Stage 2 Gate Voltage		-3.925		V
Stage 1 Idq		240		mA
Stage 2 Idq		960		mA

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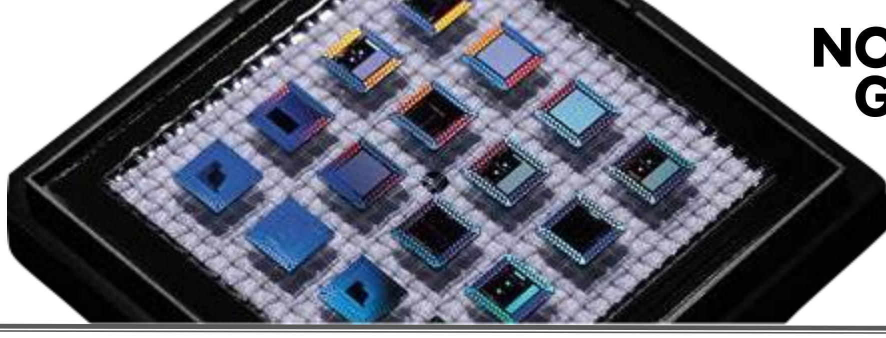

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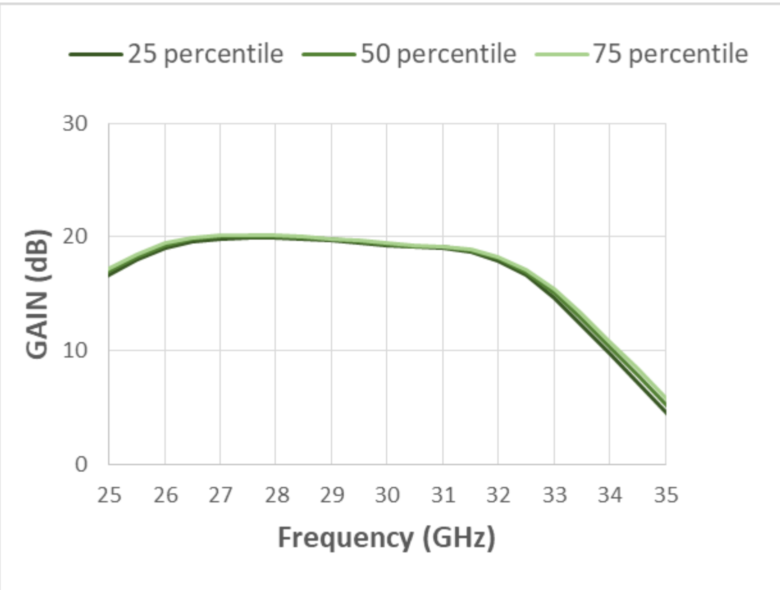
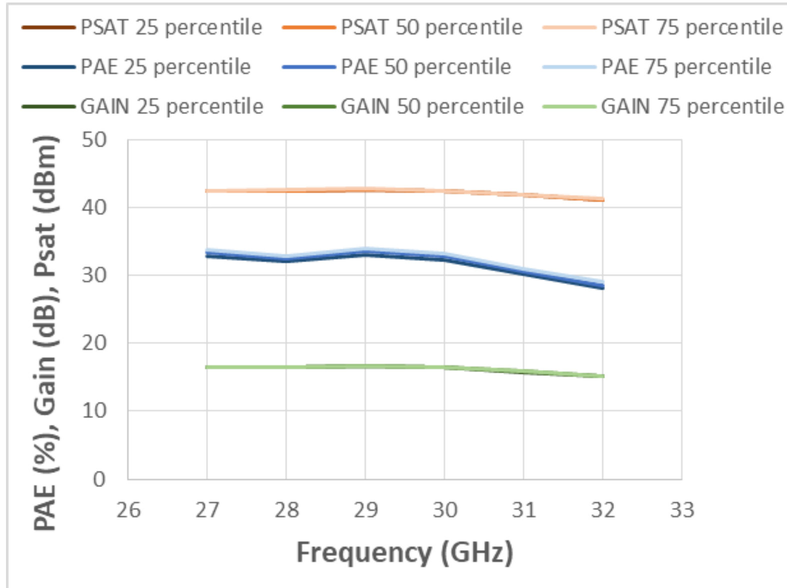
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240mA, Id2 + Id2a =960 mA

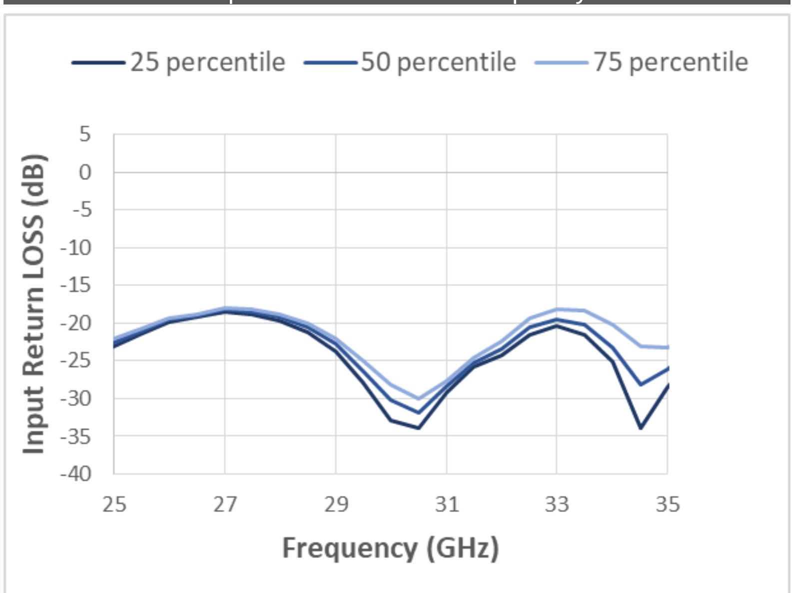
Small Signal GAIN vs. Frequency



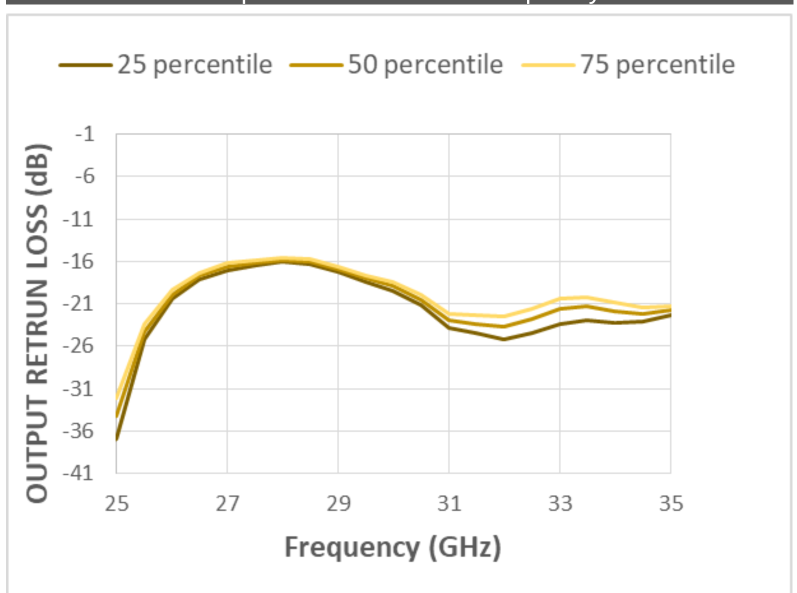
Large Signal PAE, GAIN, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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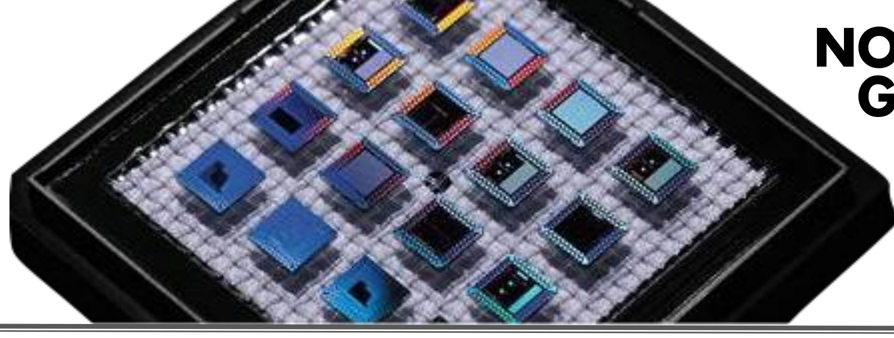

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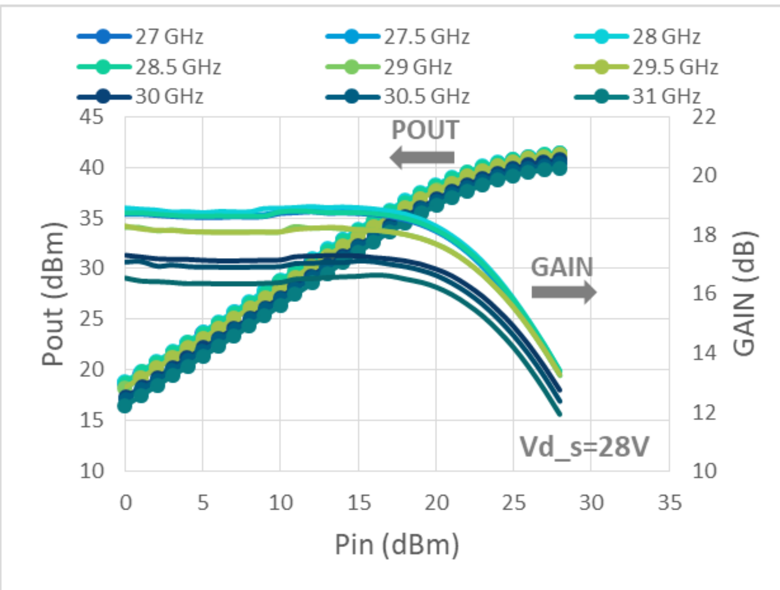
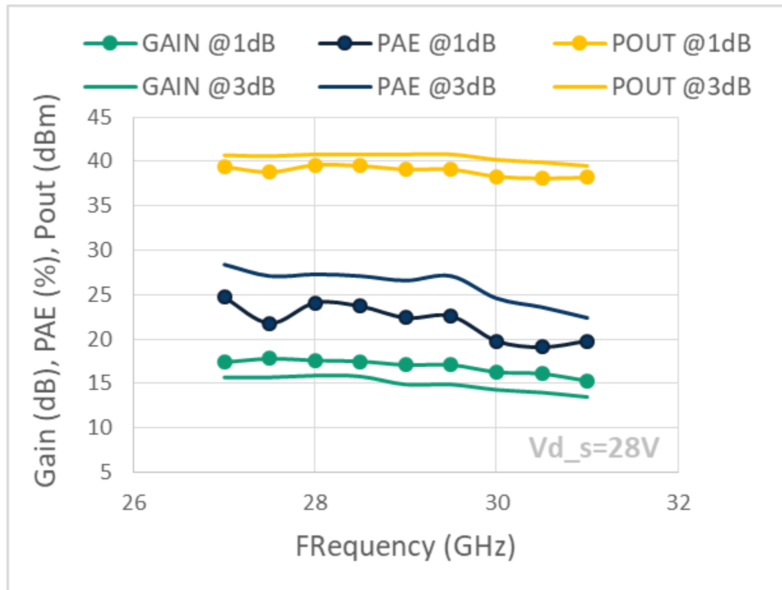
Fixture measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240mA, Id2 + Id2a =960 mA

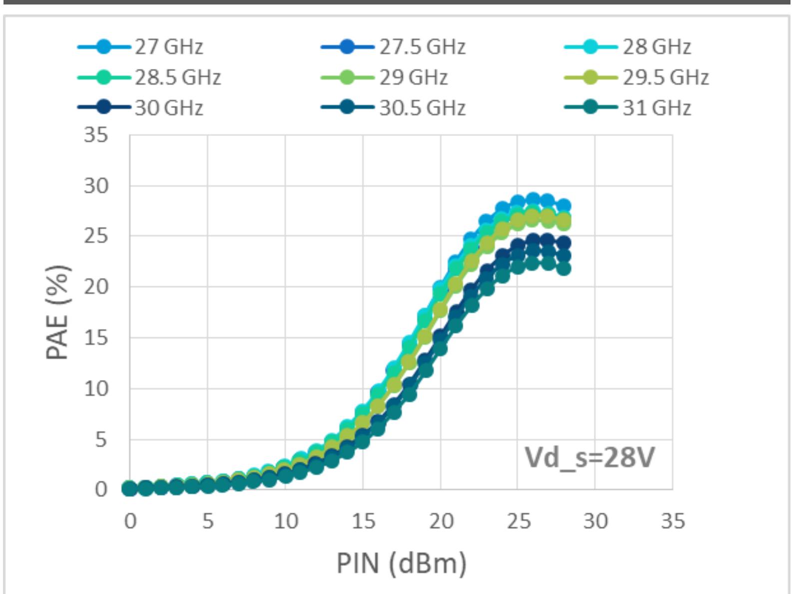
POUT and GAIN vs. PIN



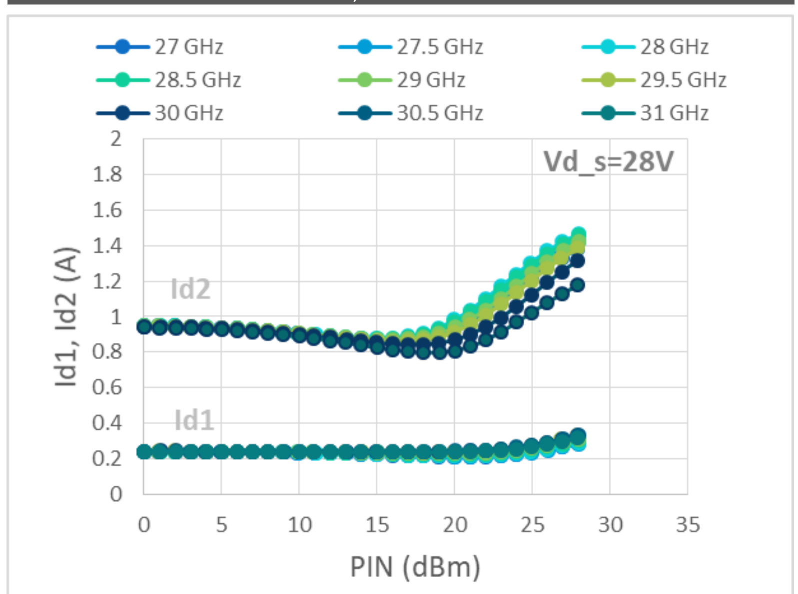
PAE, GAIN, POUT vs. FREQUENCY



PAE vs PIN



Id1, Id2 vs PIN



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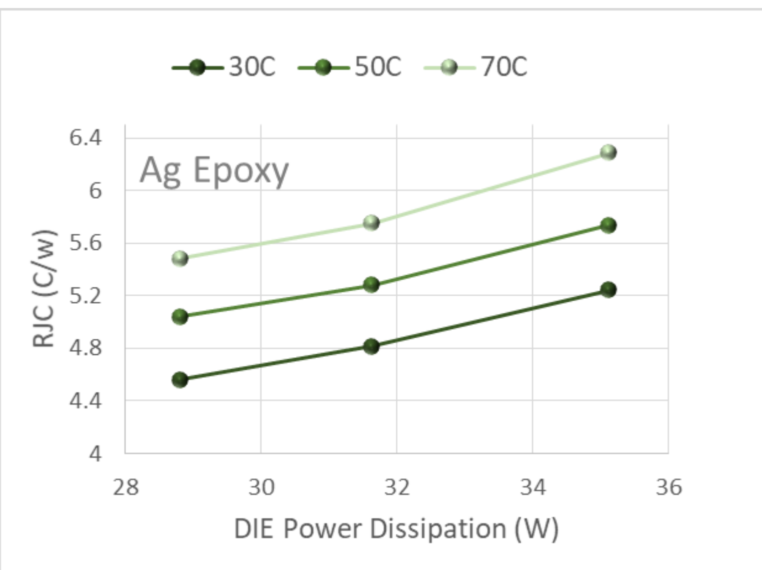
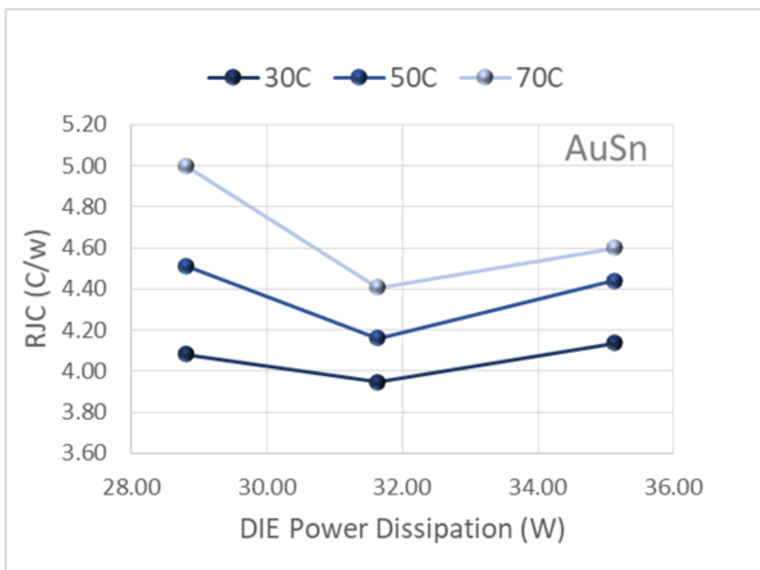
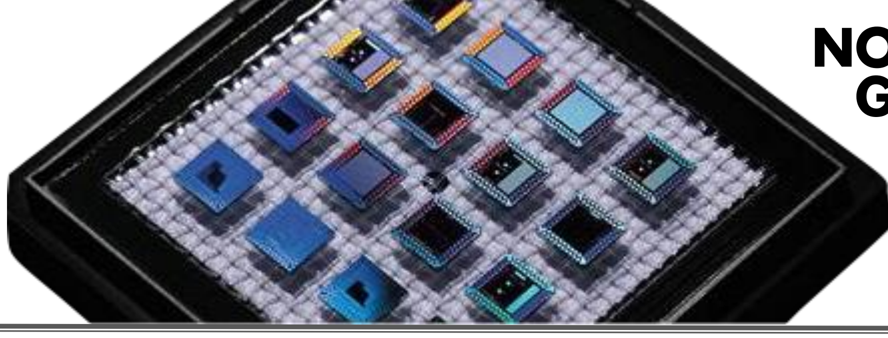
Preliminary Thermal Properties with die mounted with 25um 80/20 AuSn Eutectic to: 10mil Cu10W Shim.

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature Tjc	RF Output (dBm)	Power Dissipation (W)	Thermal Resistance Rjc (ºC/W)
10 mil CuW	AuSn Eutectic	50 ºC	147	39.8	28.81	4.08
			155	41.0	31.64	3.95
			175	41.3	35.13	4.14
		70 ºC	180	39.8	28.81	4.51
			181	41.0	31.64	4.16
			206	41.3	35.13	4.44
		90 ºC	213	39.8	28.81	4.95
			209	41.0	31.64	4.40
			218	41.3	35.13	4.22
10 mil CuW	Ag Epoxy	30 ºC	161	39.8	28.81	4.56
			182	41.0	31.64	4.82
			214	41.3	35.13	5.24
		50 ºC	195	39.8	28.81	5.04
			217	41.0	31.64	5.28
			251	41.3	35.13	5.73
		70 ºC	228	39.8	28.81	5.48
			252	41.0	31.64	5.75
			291	41.3	35.13	6.29



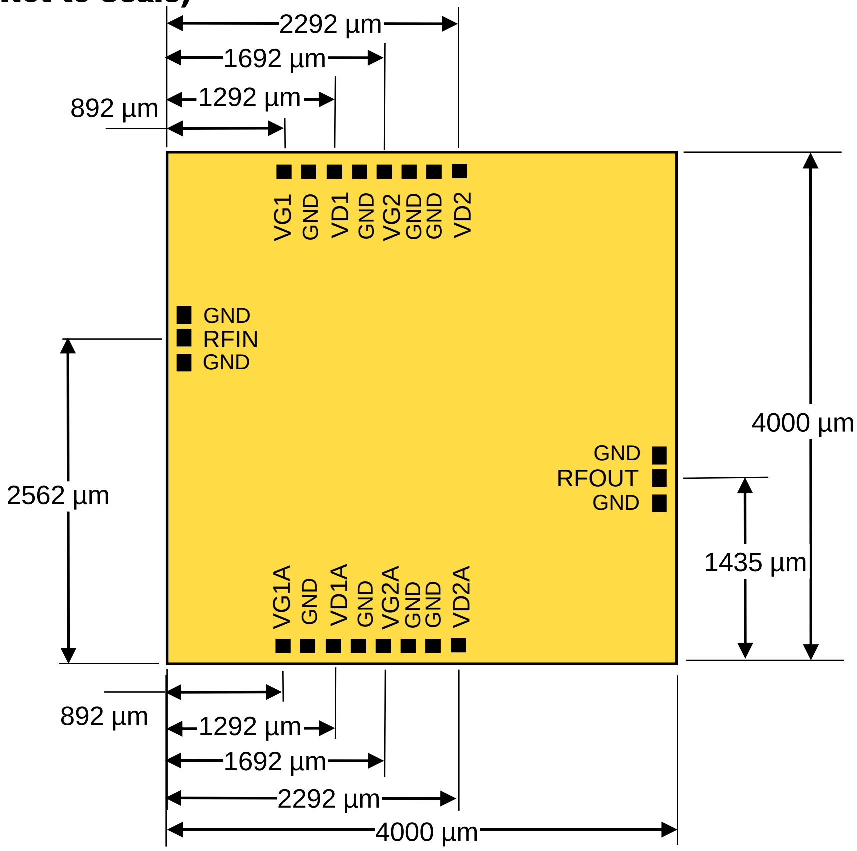


** Vd = 28.0 V, Idq1 = 240 mA, Id2q = 960 mA



Die Size and Bond Pad Locations (Not to Scale)

X = 4000 µm ± 25 µm
Y = 4000 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

Bias for 1st stage is from top. The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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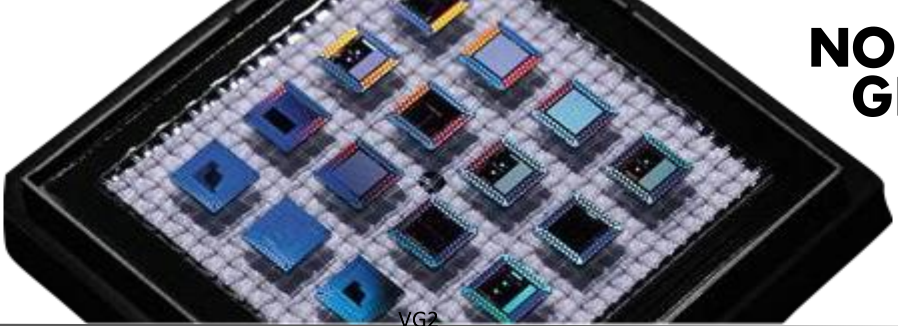

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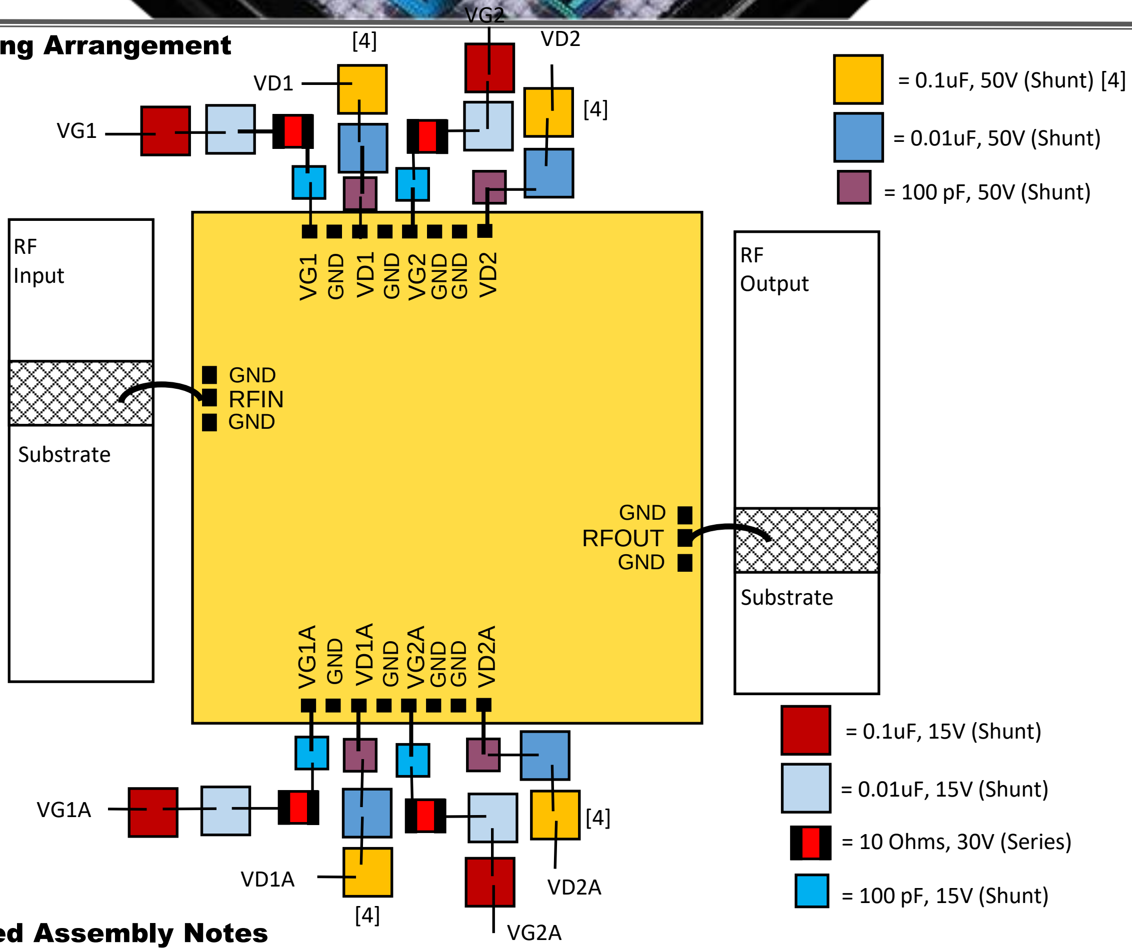
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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