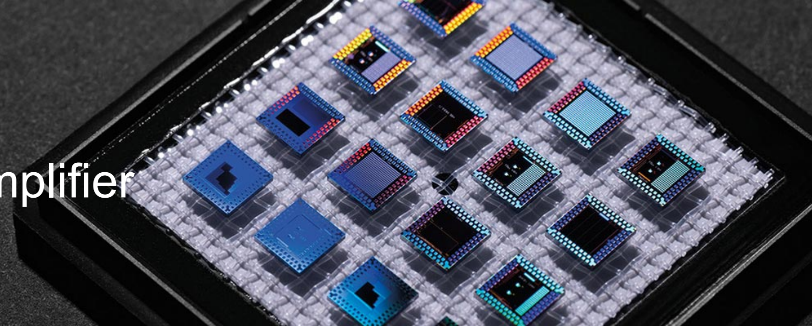
APN250
10-14 GHz
GaN Driver Amplifier



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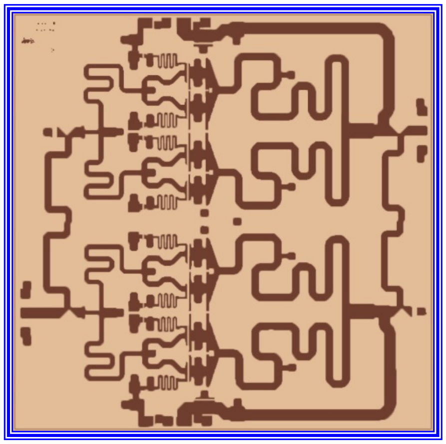

X = 4.3 mm Y = 4.3 mm

Product Features

- RF frequency: 10 to 14 GHz
- Linear Gain: 13 typ.*
- P1dB: 39 dBm typ.*
- Psat: 42 dBm typ.*
- PAE% @ Psat: 37% typ.*
- Die Size: 18.5 sq. mm
- 0.2 um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 24 VDC @ 1280 mA

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- VSAT
- Test Instrumentation

Product Description

The APN250 monolithic GaN HEMT amplifier is a broadband, balanced Single Stage power device, designed for use in SATCOM Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	10		14	GHz
Linear Gain	12	13		dB
Input Return Loss	20	25		dB
Output Return Loss	20	25		dB
P1dB (PP*)		39		dBm
Psat (PP*)	40.5	42		dBm
PAE @ Psat (PP*)		37		%
Pgain @ Pin=32dB		9.5		dB
Vd1,Vd2		22		V
Vg1, Vg2		-3.5		V
Id1		640		mA
Id1a		640		mA

* Pulsed Power on-Wafer

Export Information
ECCN: **5A991.g**
HTS (Schedule B) code: **8542.33.0000**

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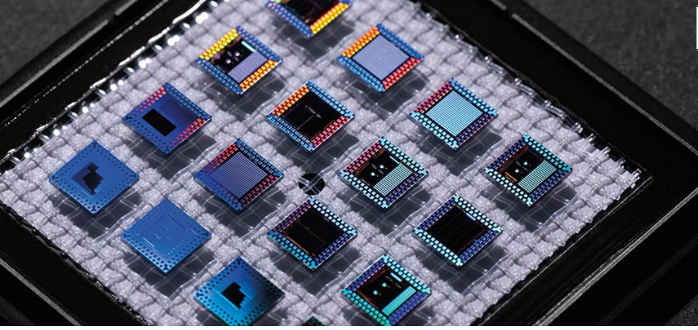

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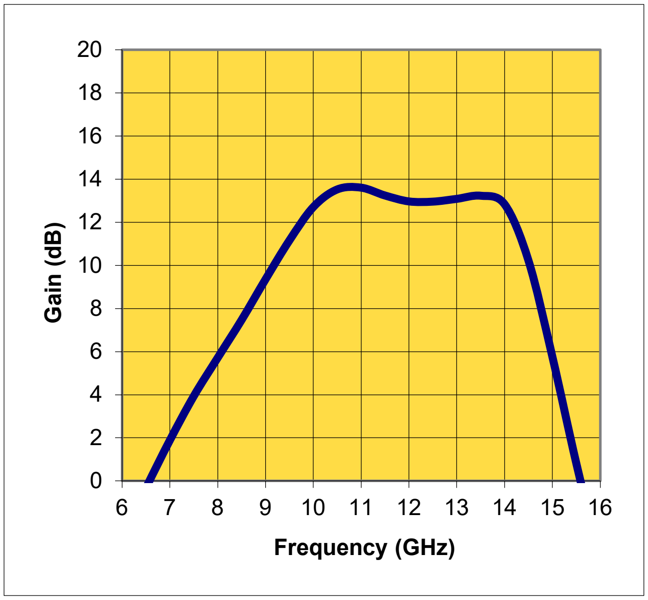
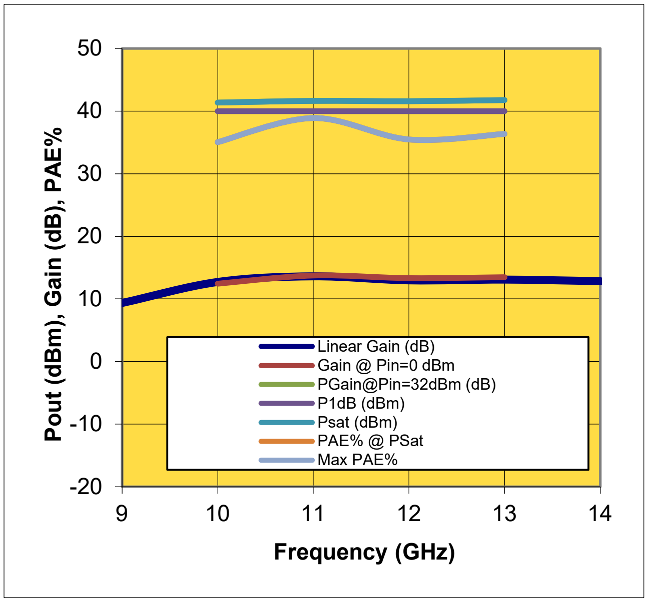
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 640 mA, Id1a = 640 mA. *

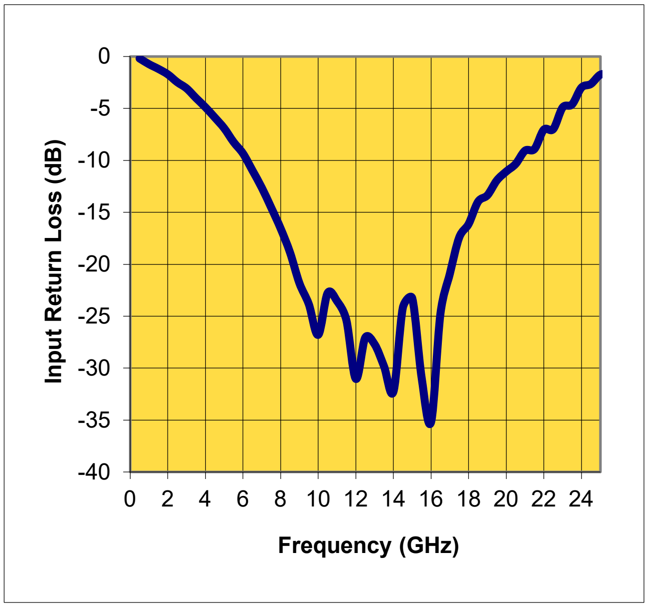
GAIN vs. Frequency



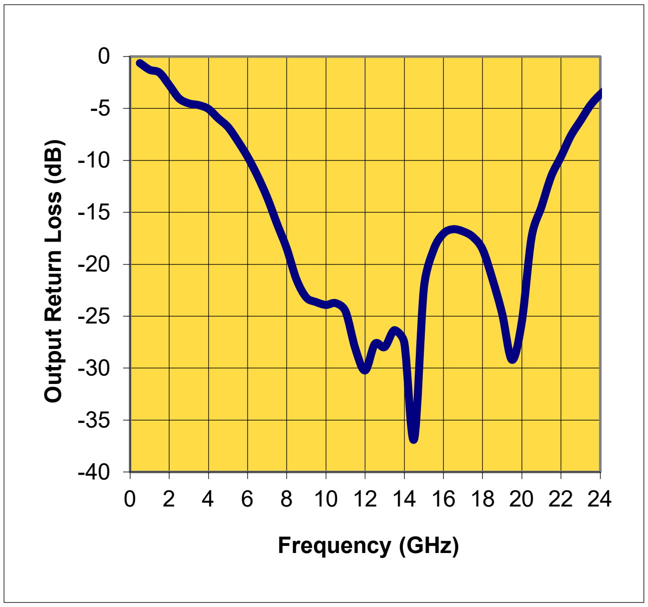
PAE, GAIN, Pout vs. Frequency **



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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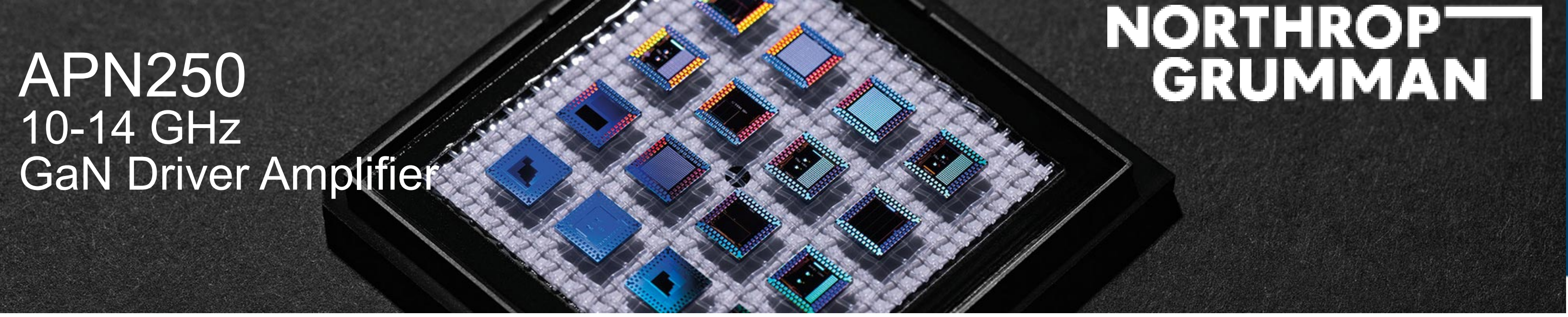

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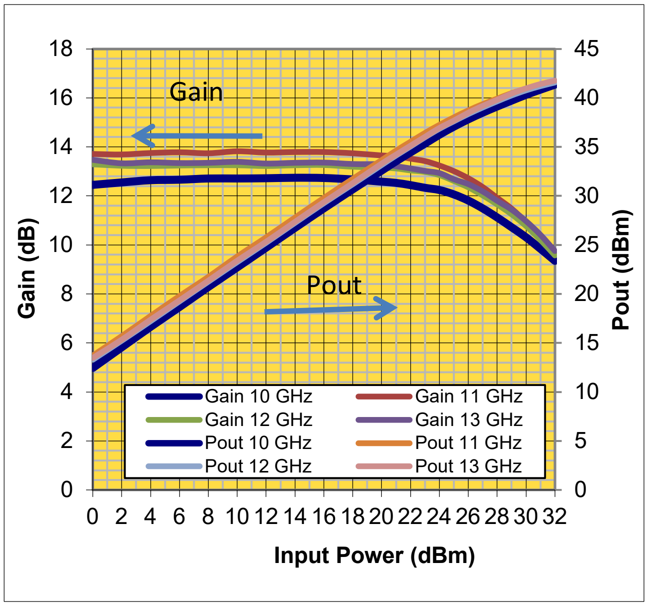
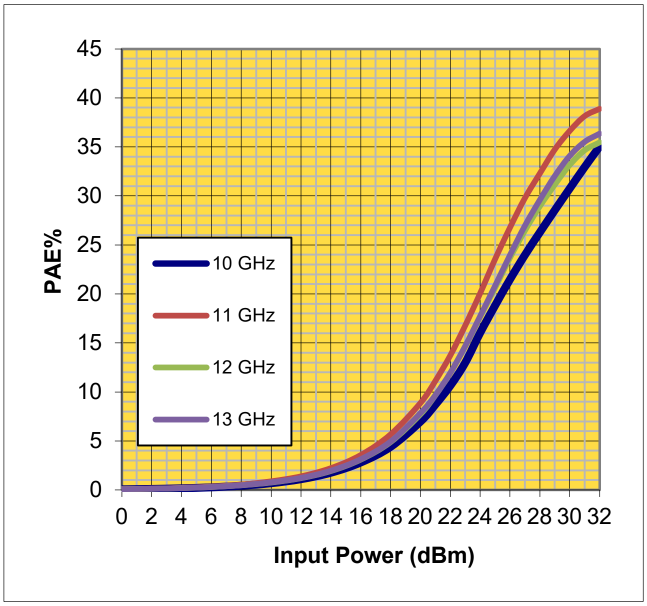
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 640 mA, Id1a = 640 mA.*

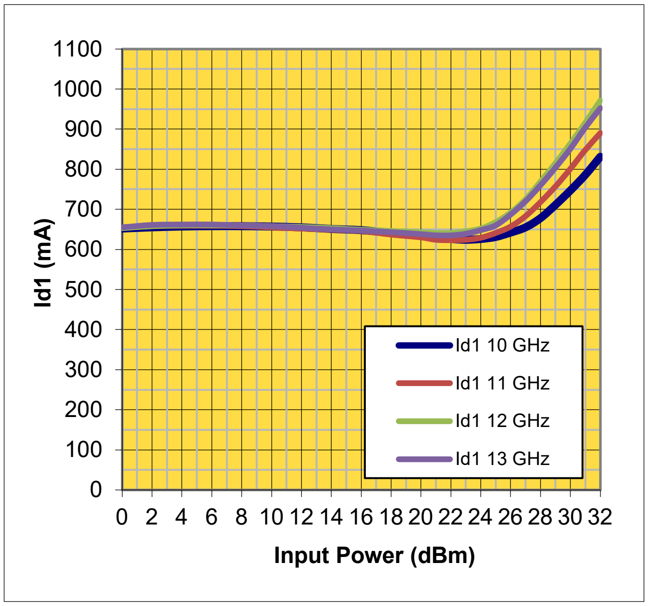
GAIN, Pout vs. Pin



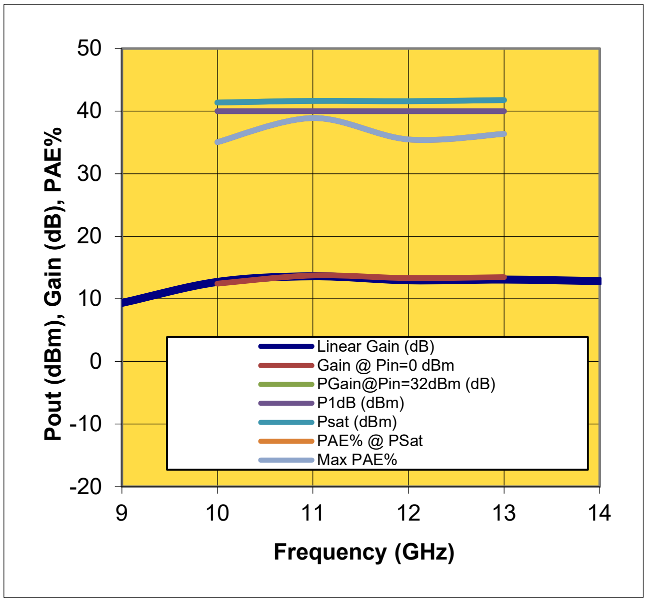
PAE vs. Pin



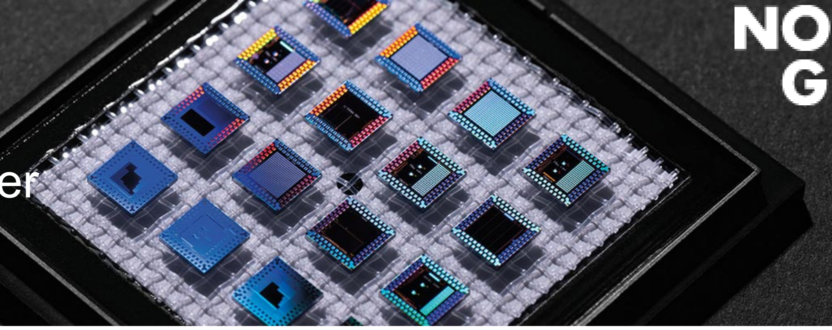
Id vs Pin



Pout, Gain, PAE vs. Frequency



*Pulsed-power on-wafer



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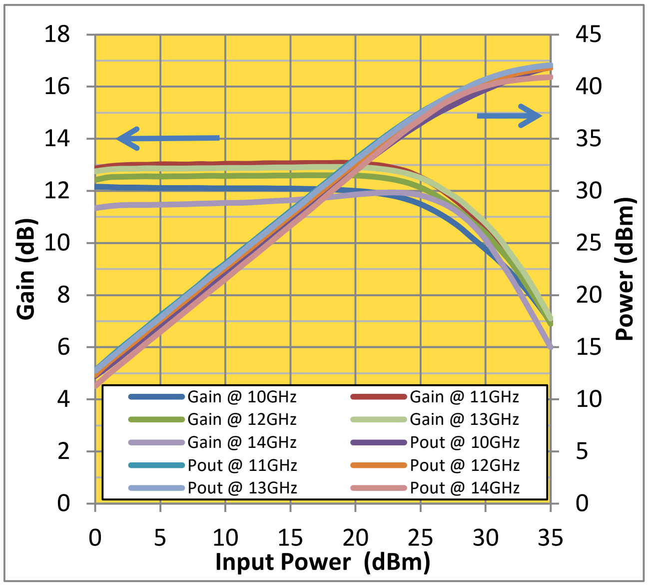
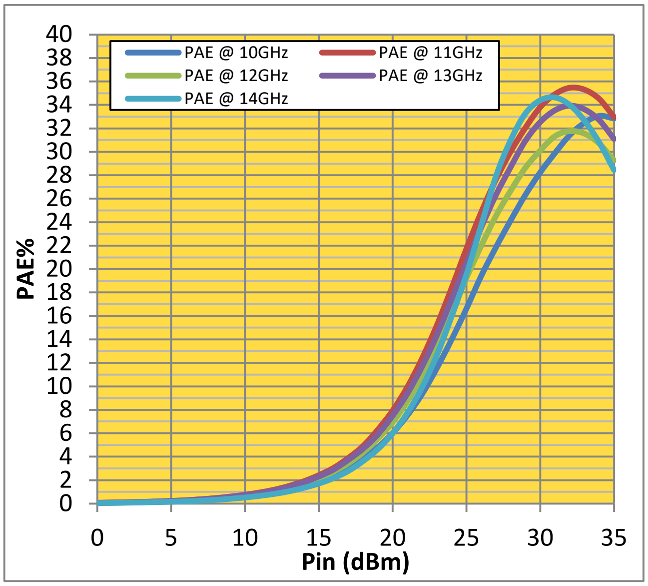
Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 20 V, Id= Id1+ Id1a= 1280 mA.

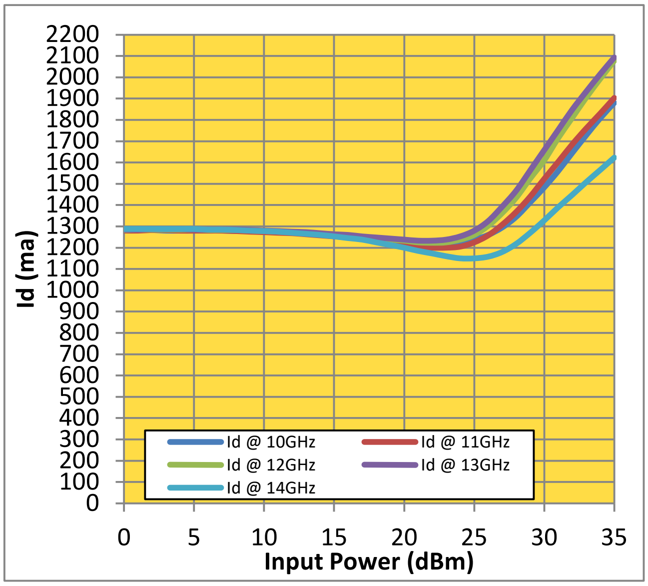
GAIN, Pout vs. Pin



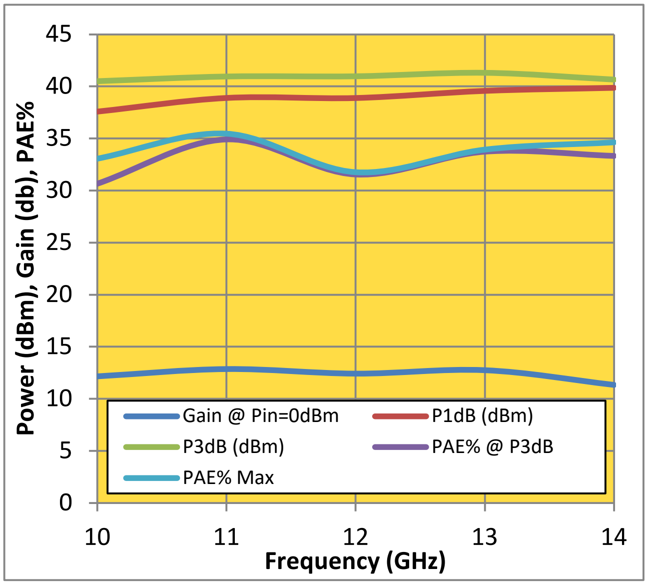
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



** CW fixtured

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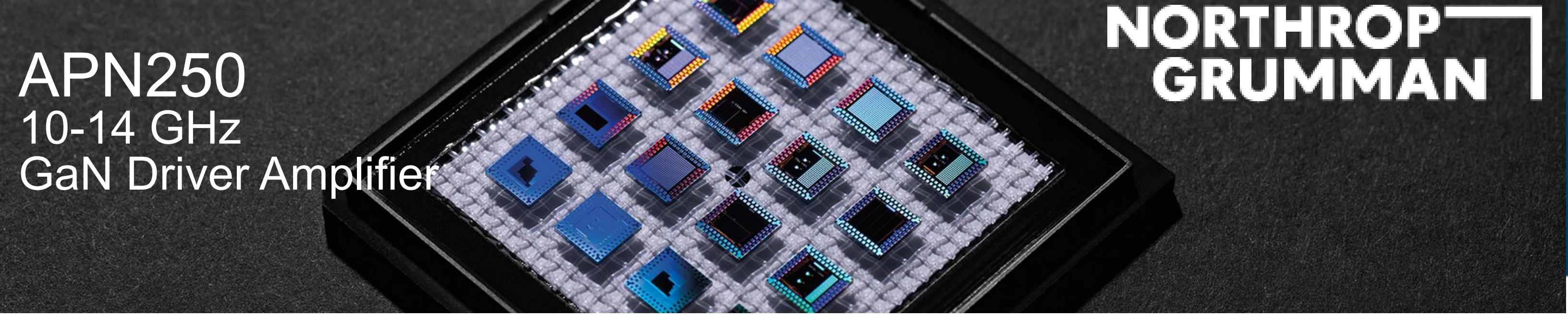

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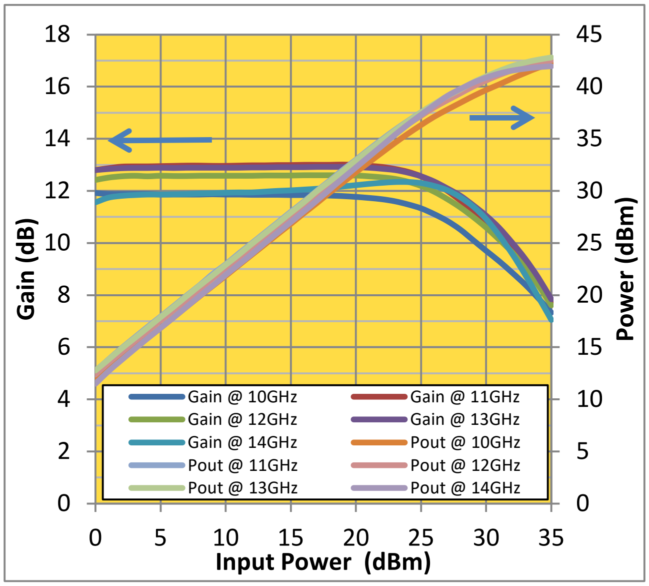
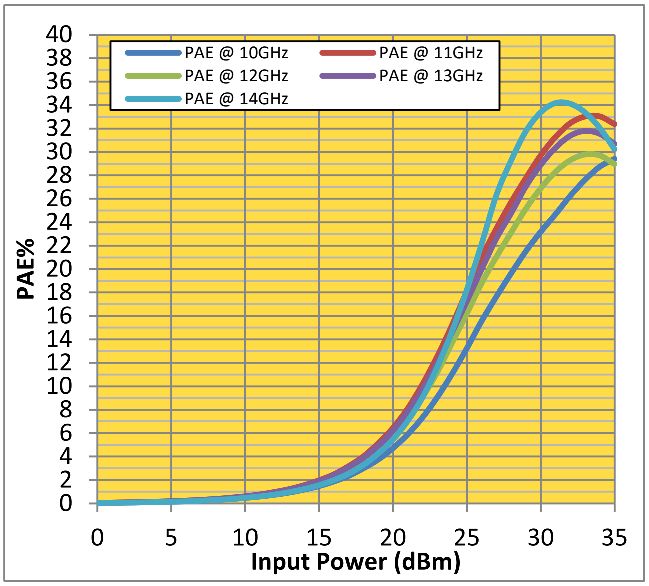
Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 24 V, Id = Id1+ Id1a = 1280 mA.*

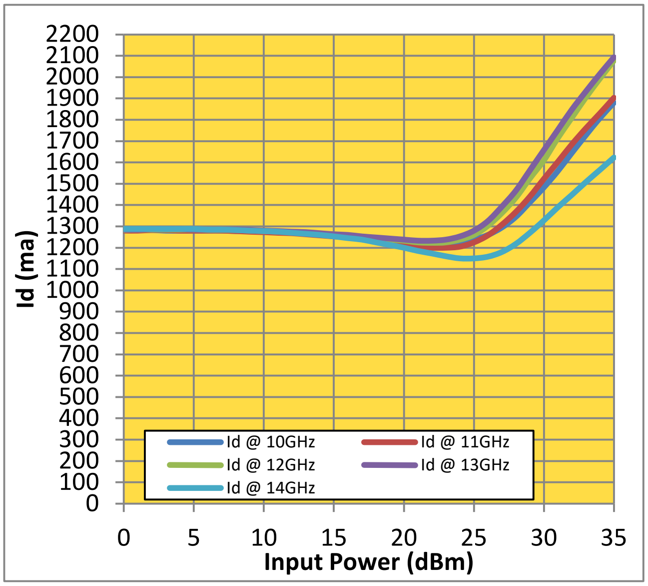
GAIN, Pout vs. Pin



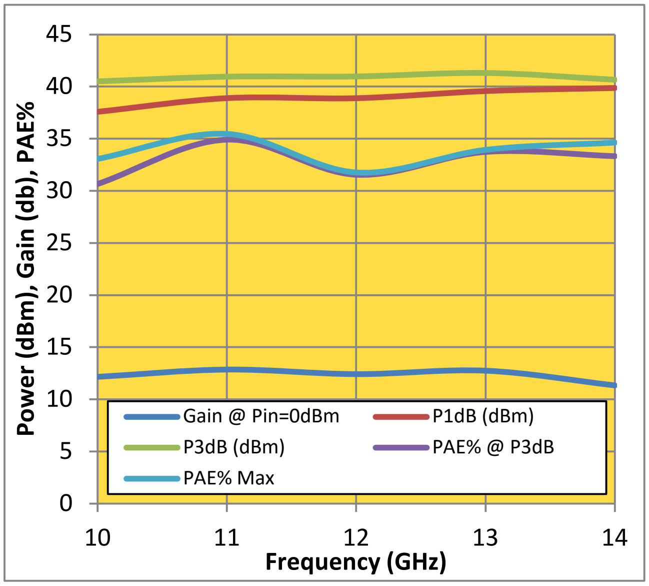
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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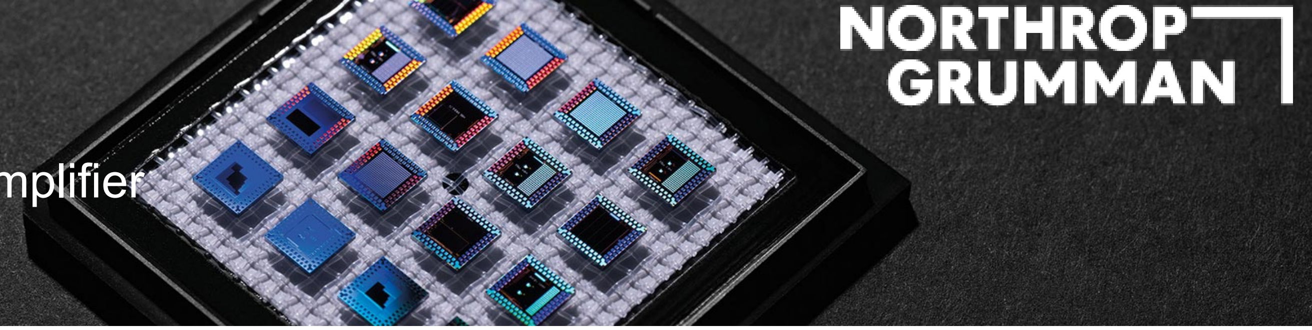

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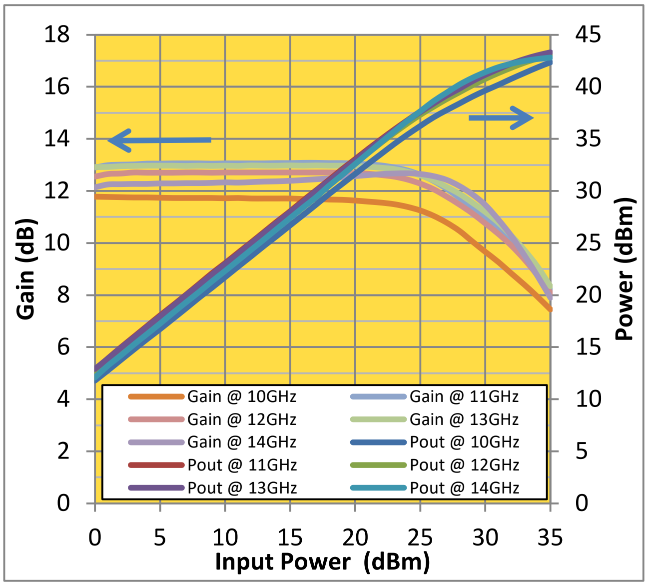
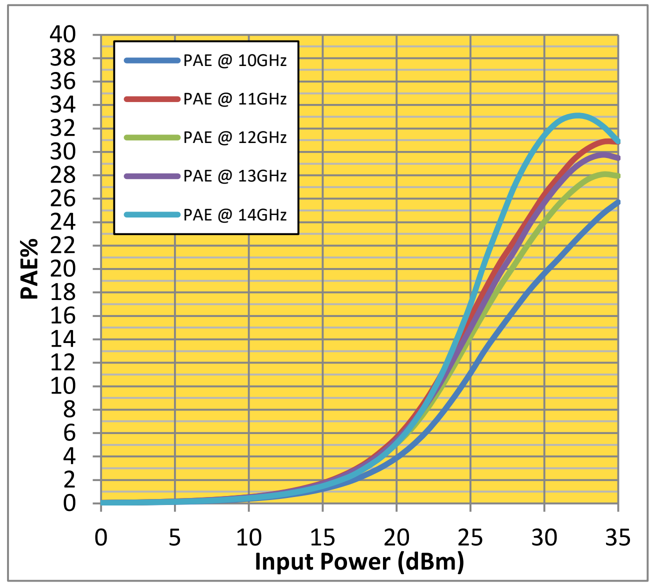
Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 28 V, Id = Id1+ Id1a = 1280 mA.*

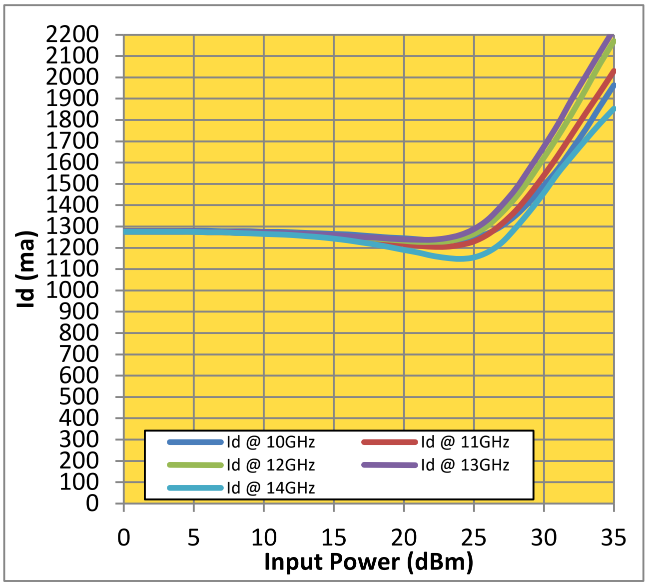
GAIN, Pout vs. Pin



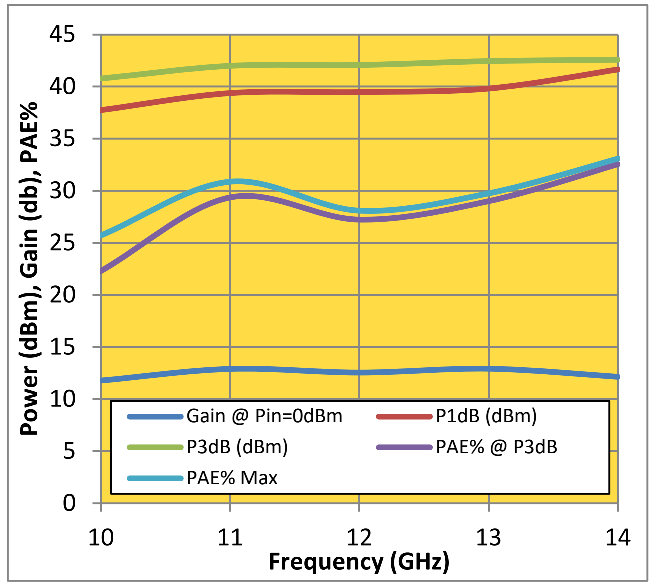
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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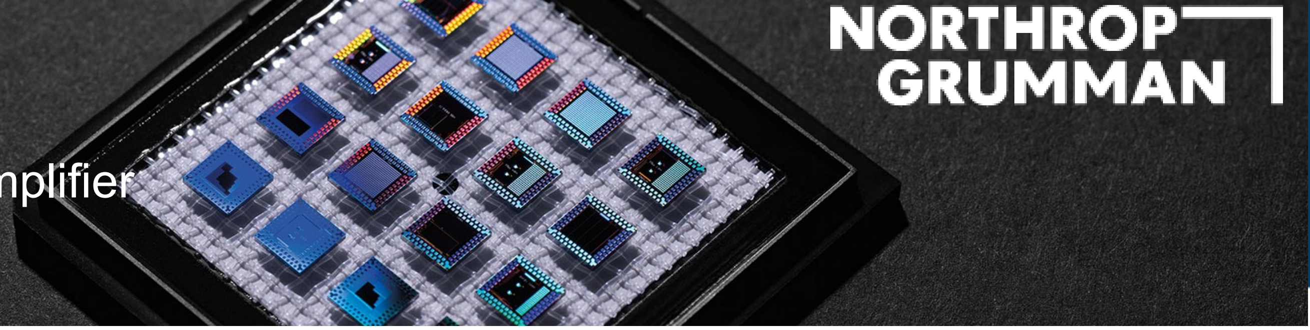

On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 640 mA, Id1a = 640 mA. *

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
2.0	0.820	-65.461	0.065	-106.660	0.002	155.653	0.716	-179.860
2.5	0.754	-81.017	0.131	-127.922	0.004	-153.056	0.605	161.581
3.0	0.701	-95.289	0.187	-162.120	0.005	75.662	0.590	148.317
3.5	0.629	-108.778	0.222	174.631	0.002	-18.762	0.587	130.937
4.0	0.566	-123.725	0.268	155.688	0.002	140.685	0.566	114.786
4.5	0.498	-138.593	0.338	136.618	0.006	92.027	0.510	97.370
5.0	0.440	-152.317	0.434	117.681	0.006	53.131	0.469	79.660
5.5	0.372	-166.123	0.570	96.851	0.006	32.327	0.405	62.223
6.0	0.323	179.670	0.760	74.152	0.012	1.995	0.345	44.786
6.5	0.262	164.893	0.991	48.828	0.012	-39.117	0.288	27.393
7.0	0.221	151.577	1.278	21.180	0.017	-58.088	0.228	9.534
7.5	0.178	134.537	1.609	-8.032	0.020	-89.071	0.178	-8.533
8.0	0.147	122.335	1.971	-37.638	0.023	-115.822	0.136	-27.674
8.5	0.117	93.874	2.412	-67.898	0.032	-146.204	0.098	-47.492
9.0	0.095	73.743	2.991	-99.133	0.047	-177.428	0.077	-77.161
9.5	0.097	27.863	3.683	-133.826	0.061	151.774	0.063	-108.207
10.0	0.070	-14.142	4.429	-172.232	0.072	107.605	0.062	-142.100
10.5	0.087	-54.384	4.884	145.962	0.086	71.842	0.060	151.251
11.0	0.064	-105.853	4.953	105.050	0.093	31.185	0.064	88.753
11.5	0.050	-116.373	4.764	66.653	0.088	-4.913	0.055	30.481
12.0	0.011	-176.530	4.604	30.502	0.092	-38.570	0.042	-19.651
12.5	0.029	-87.427	4.610	-5.828	0.094	-76.291	0.042	-46.945
13.0	0.019	-106.398	4.697	-46.144	0.096	-114.334	0.044	-58.983
13.5	0.016	-61.795	4.680	-92.107	0.099	-157.632	0.056	-85.824
14.0	0.043	-29.612	4.092	-146.004	0.089	148.271	0.038	-140.276
14.5	0.064	-63.869	2.762	161.390	0.065	97.657	0.022	-2.230
15.0	0.064	-96.847	1.611	119.370	0.040	54.150	0.082	-55.593
15.5	0.015	-139.357	0.922	86.830	0.021	22.202	0.109	-87.029
16.0	0.023	-26.789	0.553	60.210	0.018	-3.703	0.128	-109.362
16.5	0.074	17.693	0.344	36.828	0.010	-11.102	0.132	-128.407
17.0	0.092	-21.030	0.221	16.314	0.007	-48.648	0.133	-143.166
17.5	0.151	-20.380	0.146	-1.970	0.001	-45.067	0.122	-158.706
18.0	0.165	-42.982	0.100	-18.222	0.002	-49.744	0.108	-171.736

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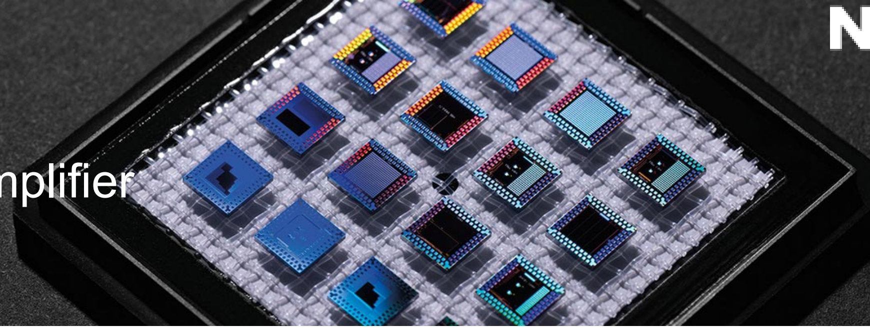
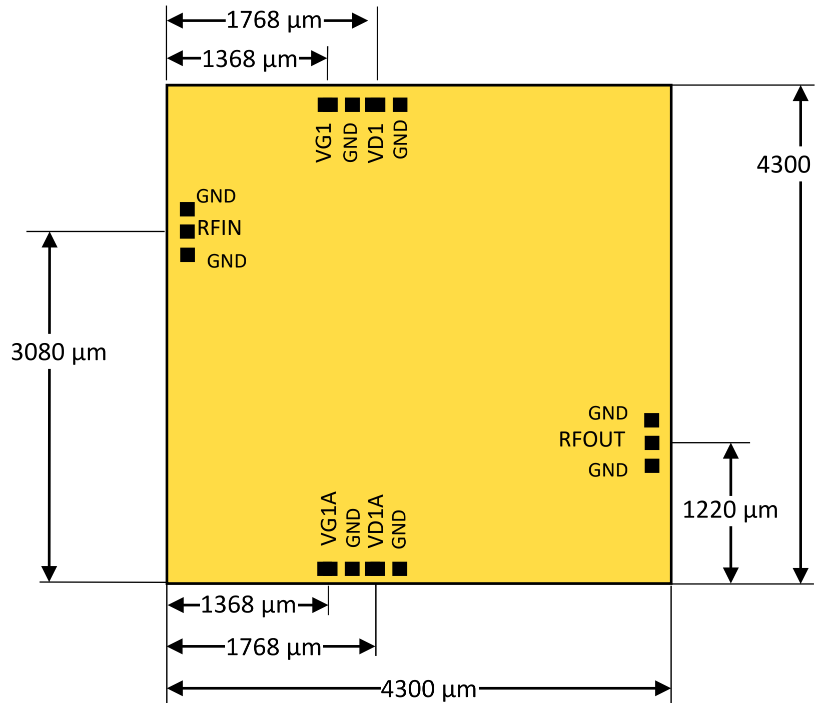


Die Size and Bond Pad Locations (Not to Scale)

X = 4300 ± 25 µm
Y = 4300 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

APN250 should be biased the top and bottom of the die. For best performance each side should be biased up separately, but they can be tied together.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
   i. Apply negative gate voltage (-5 V) to ensure that all devices are off
   ii. Ramp up drain bias to ~10 V
   iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
   iv. Ramp up drain to operating bias
   v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. Repeat bias procedure for each amplifier stage
f. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
   i. Gradually decrease drain bias to 0 V.
   ii. Gradually decrease gate bias to 0 V.
   iii. Turn off supply voltages
g. Repeat de-bias procedure for each amplifier stage

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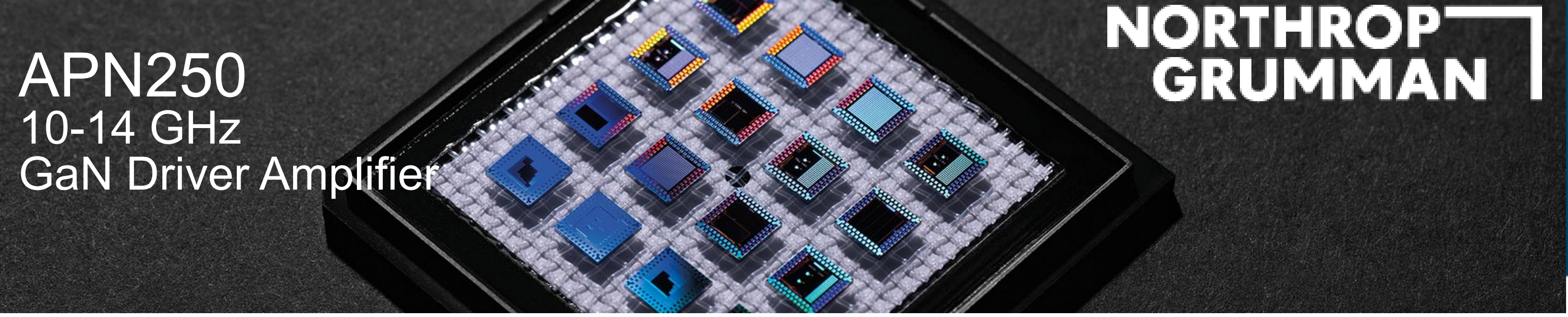

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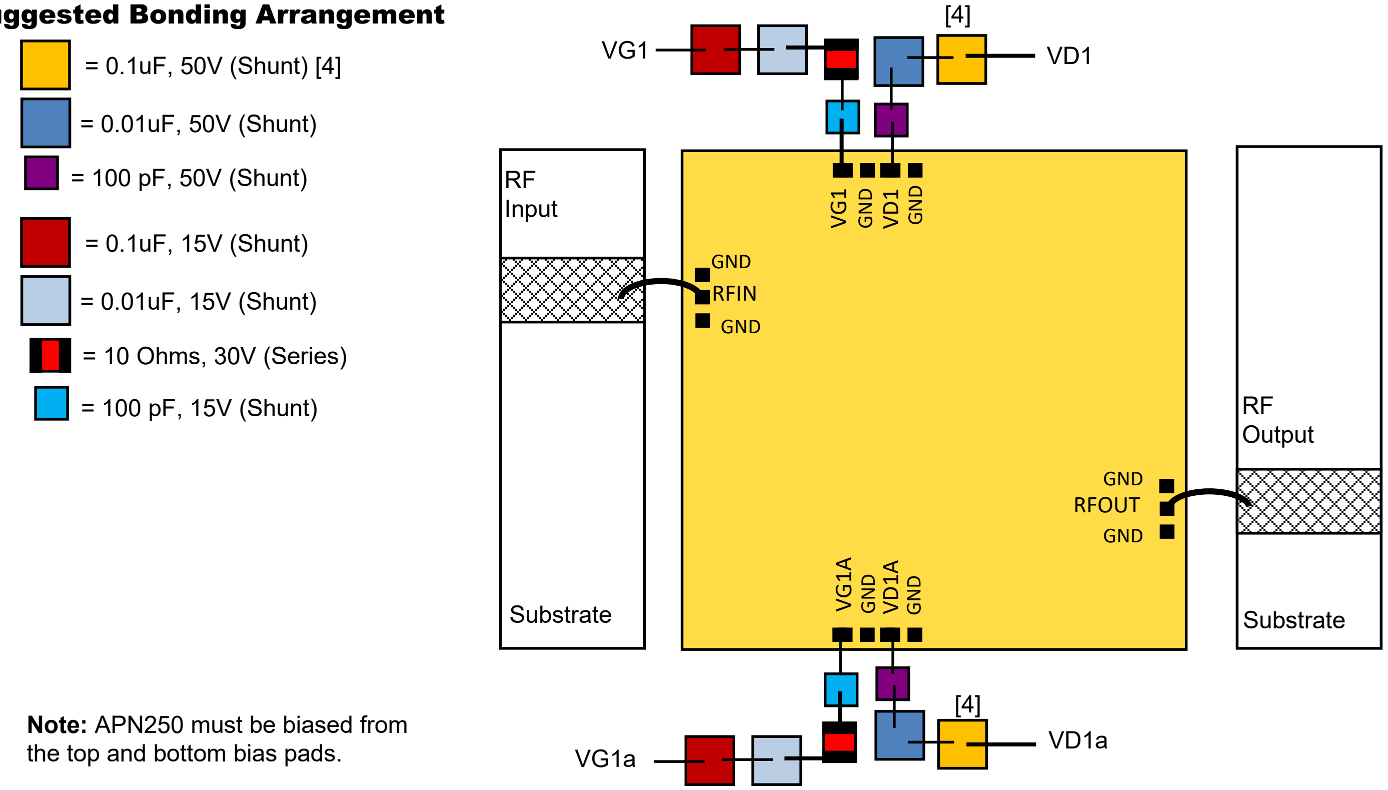
Suggested Bonding Arrangement



Note: APN250 must be biased from the top and bottom bias pads.

Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most Northrop Grumman Aerospace Systems (NGAS) GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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