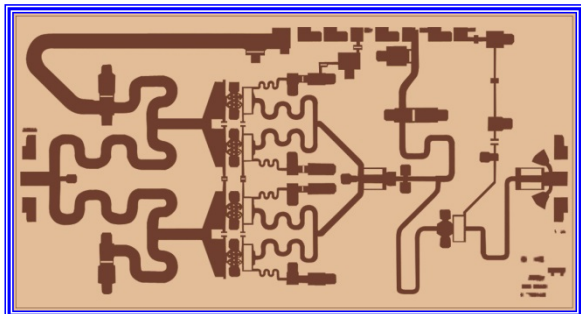
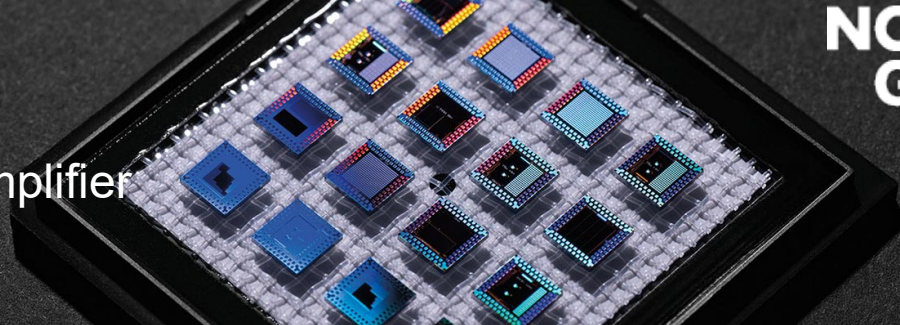


APN252 10-14 GHz GaN Driver Amplifier



X = 4.3 mm Y = 2.2 mm

Product Features

- RF frequency: 10 to 14 GHz
- Linear Gain: 25.5 typ.*
- P1dB: 34 dBm typ.*
- Psat: 38 dBm typ.*
- PAE% @ Psat: 40% typ.*
- Die Size: 9.46 sq. mm
- 0.2 um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 24 VDC @ 480 mA

Export Information

ECCN: 5A991.g

HTS (Schedule B) code: 8542.33.0000

Applications

- Electronic Warfare
- Radar
- Test Equipment

Product Description

The APN252 monolithic GaN HEMT amplifier is a broadband, 2 Stage power device, designed for use in SATCOM Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

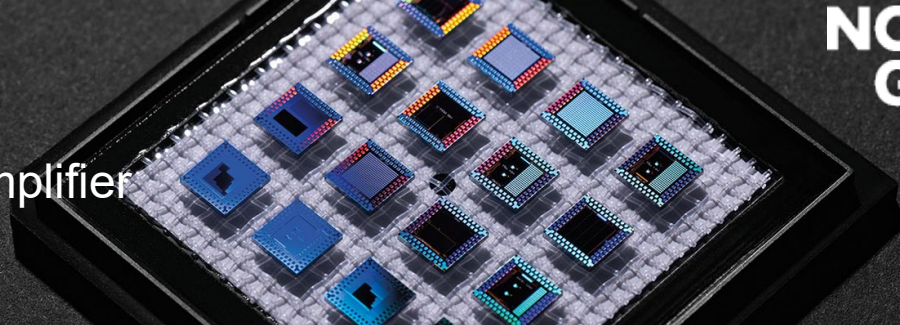
Specification	Min	Typ	Max	Unit
Frequency	10		14	GHz
Linear Gain	23	25.5		dB
Input Return Loss	10	18		dB
Output Return Loss	2	3		dB
P1dB (PP*)		34		dBm
P1dB (CW**)		34		dBm
Psat (PP*)	37	38		dBm
Psat (CW**)		37.5		dBm
PAE @ Psat (PP*)		40		%
PAE @ Psat (CW**)		32		%
Max PAE (PP*)		42		%
Max PAE (CW)		34		%
Vd1, Vd2		22		V
Vg1, Vg2		-3.5		V
Id1		80		mA
Id2		400		mA

* Pulsed Power on-Wafer

** CW in-Fixture

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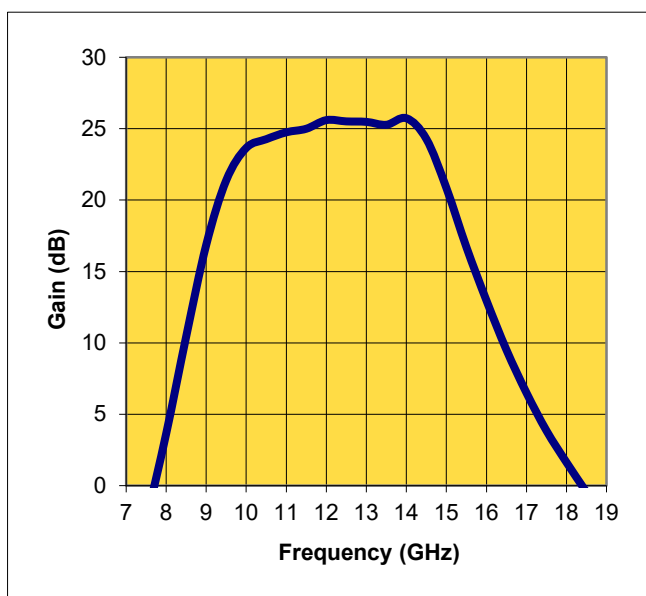
APN252 10-14 GHz GaN Driver Amplifier



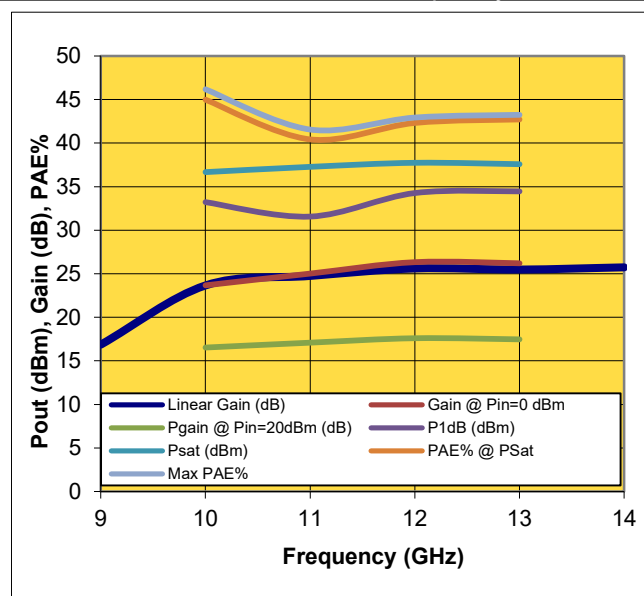
On wafer measured Performance Characteristics (Typical Performance at 25°C)

Vd1 = Vd2 = 18 V, Id1 = 80 mA, Id2 = 400 mA. *

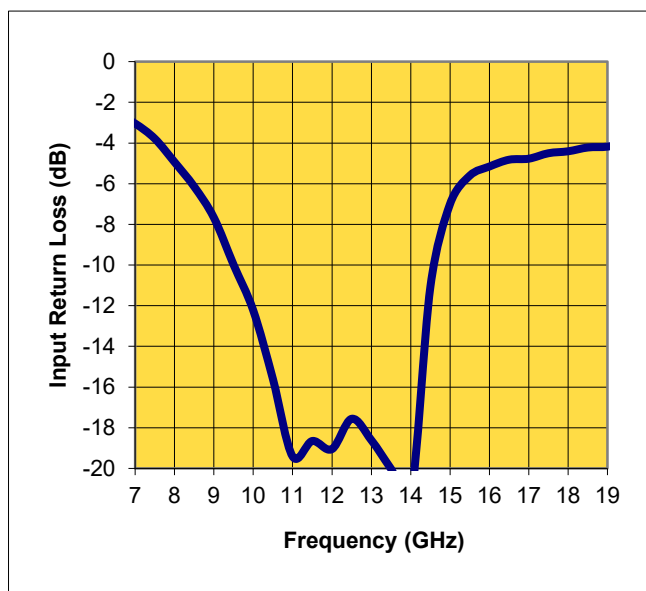
GAIN vs. Frequency



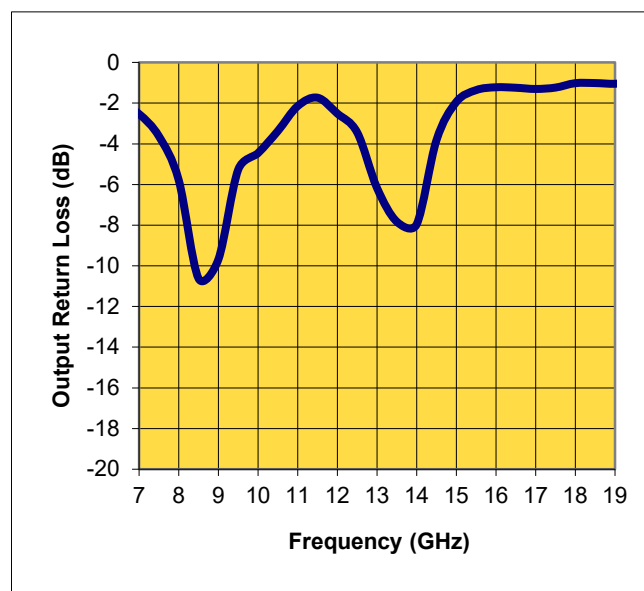
PAE, GAIN, Pout vs. Frequency **



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency

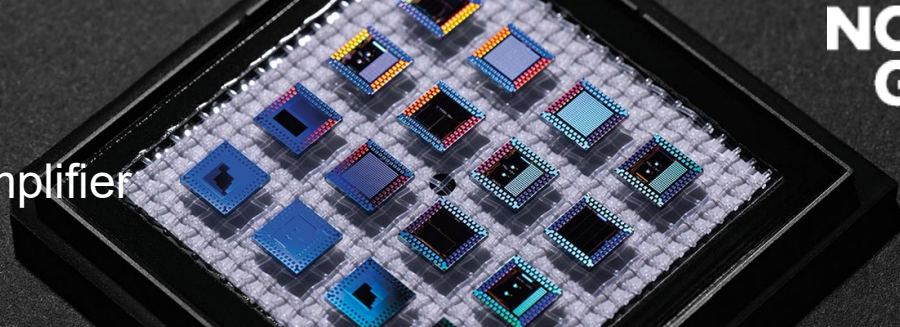


* Pulsed-power on-wafer

** CW fixtured

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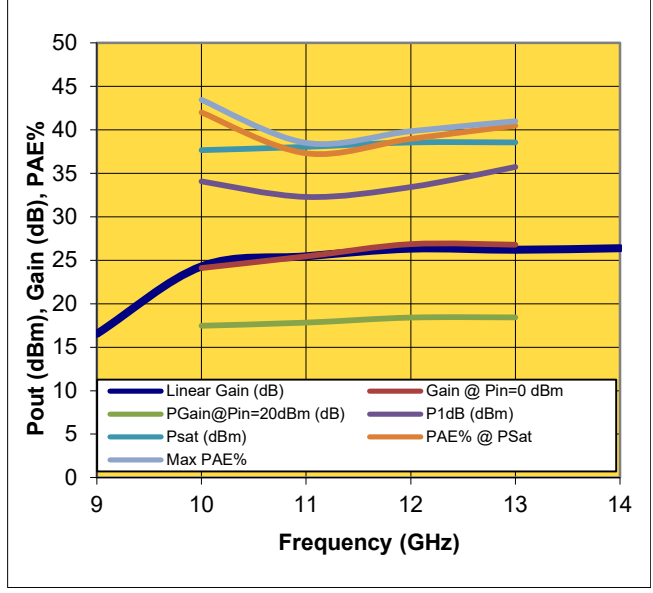
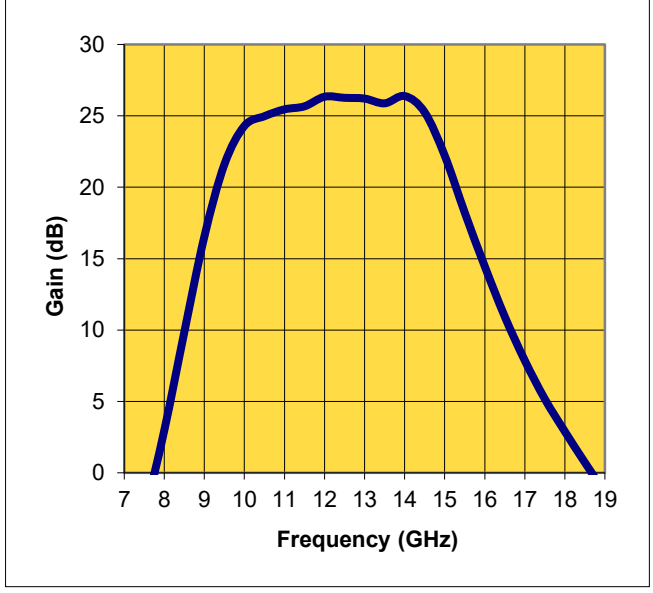
APN252 10-14 GHz GaN Driver Amplifier



On wafer measured Performance Characteristics (Typical Performance at 25°C)
 $V_{d1} = V_{d2} = 22\text{ V}$, $I_{d1} = 80\text{ mA}$, $I_{d2} = 400\text{ mA}$. *

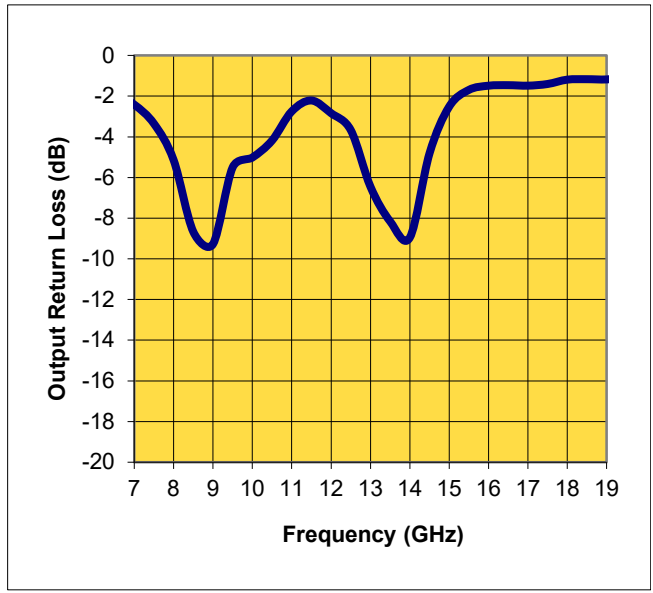
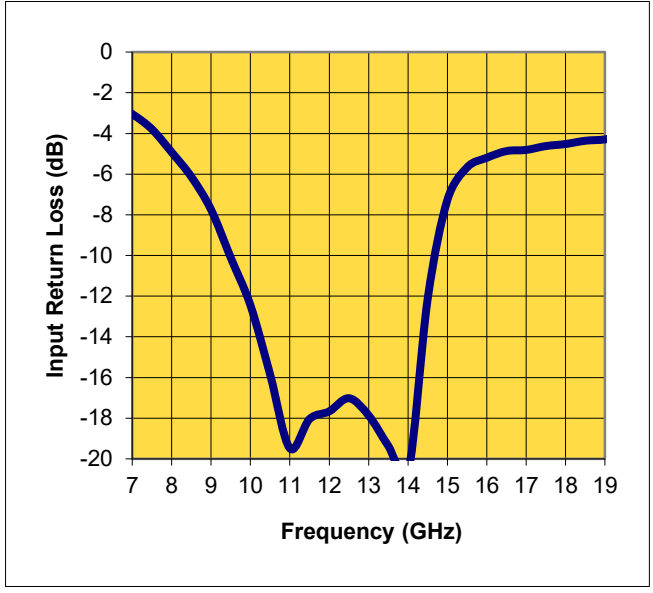
GAIN vs. Frequency

PAE, GAIN, Pout vs. Frequency **



Input Return Loss vs. Frequency

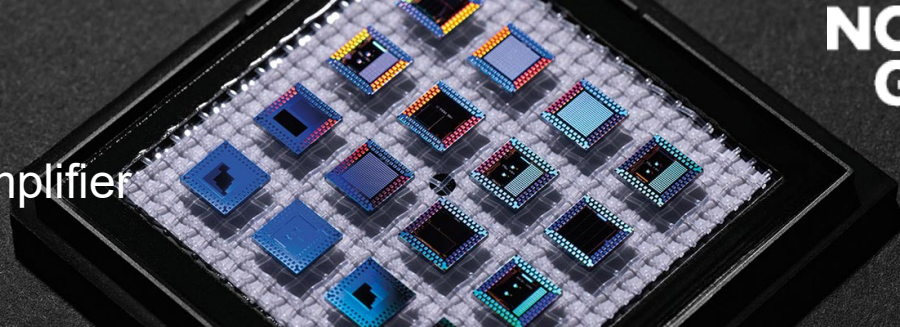
Output Return Loss vs. Frequency



* Pulsed-power on-wafer
 ** CW fixtured

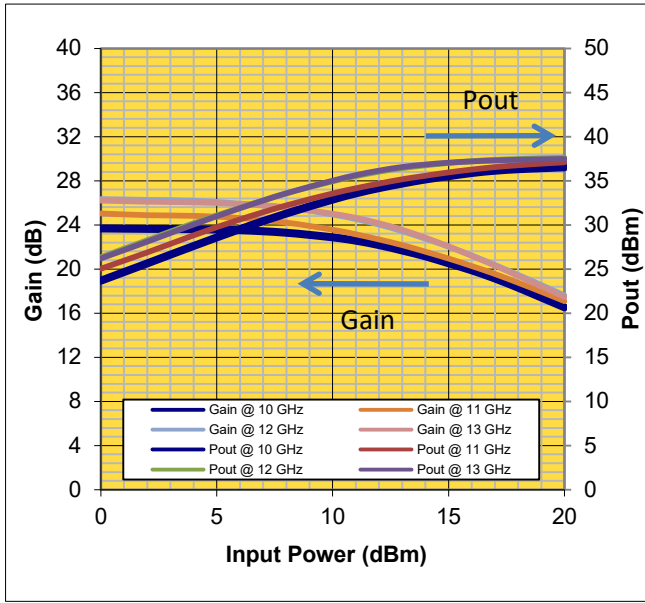
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APN252 10-14 GHz GaN Driver Amplifier

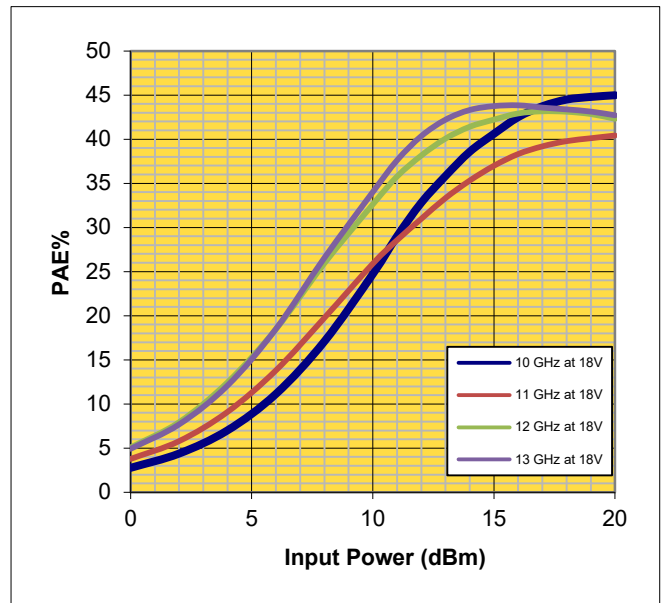


On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 18 V, Id1 = 80 mA, Id2 = 400 mA. *

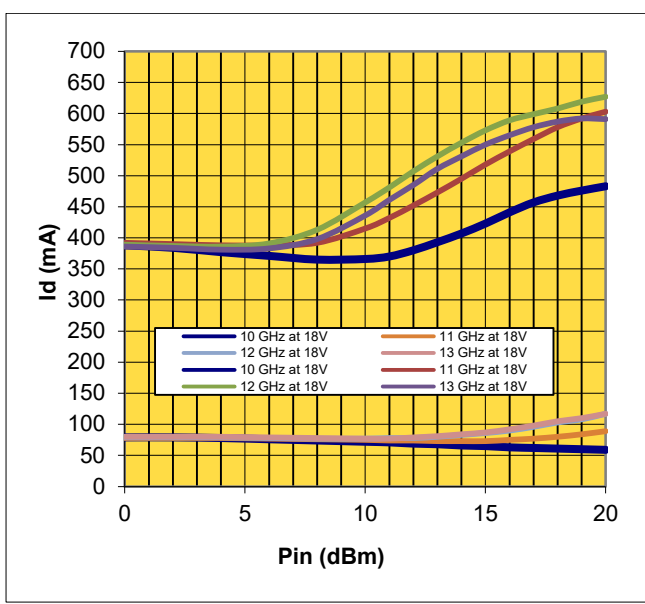
GAIN, Pout vs. Pin



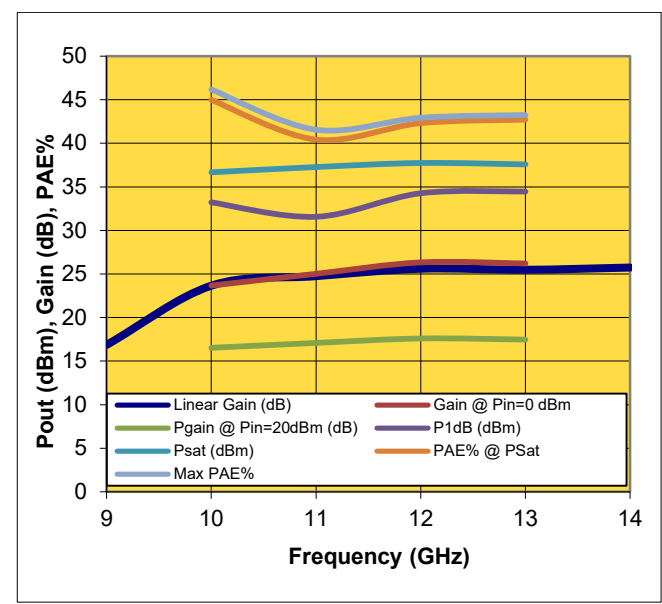
PAE vs. Pin



Id vs Pin



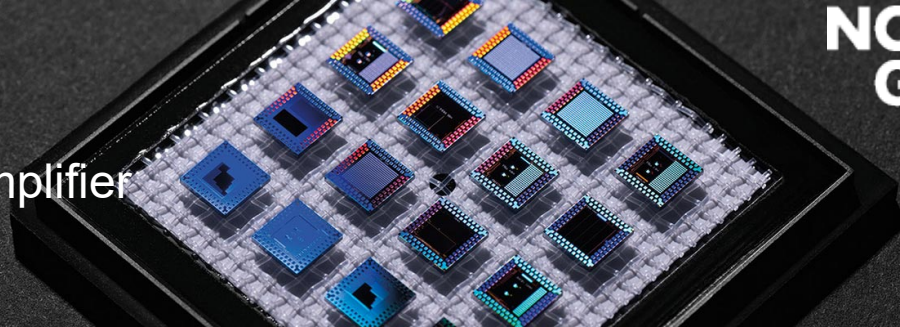
Pout, Gain, PAE vs. Frequency



*Pulsed-power on-wafer

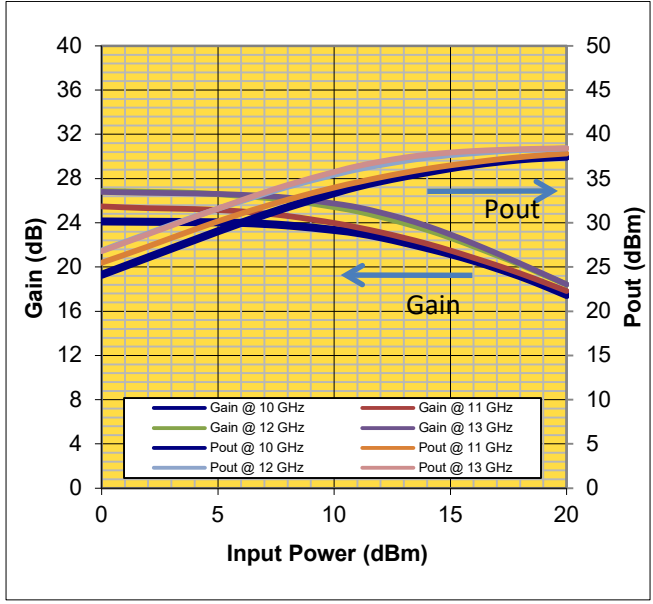
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APN252 10-14 GHz GaN Driver Amplifier

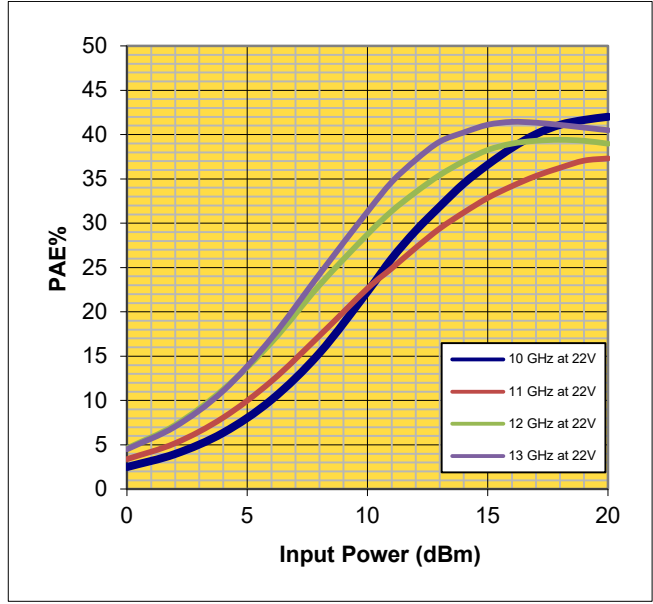


On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 80 mA, Id2 = 400 mA.

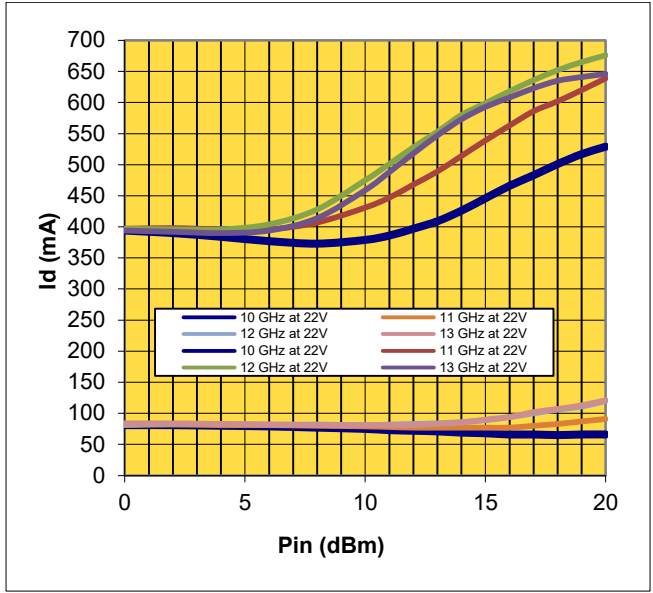
GAIN, Pout vs. Pin



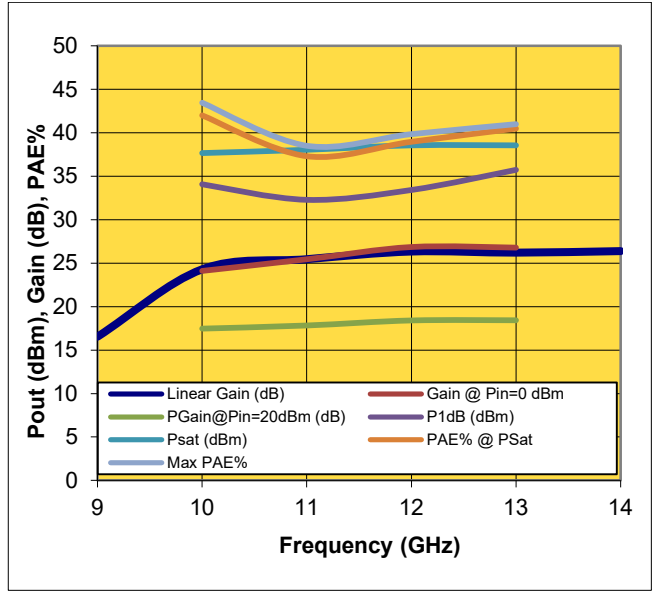
PAE vs. Pin



Id vs Pin



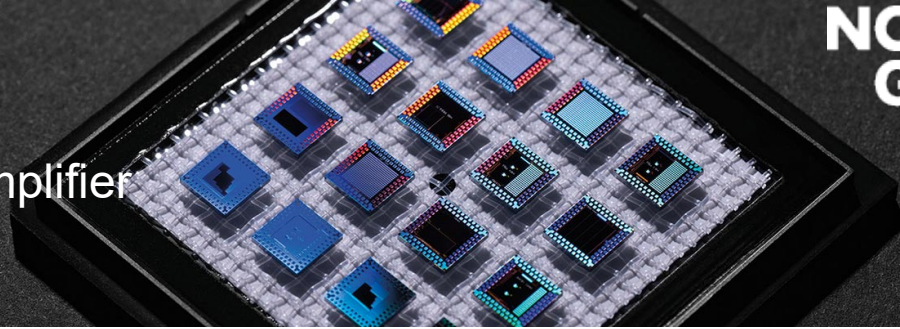
Pout, Gain, PAE vs. Frequency



*Pulsed-power on-wafer

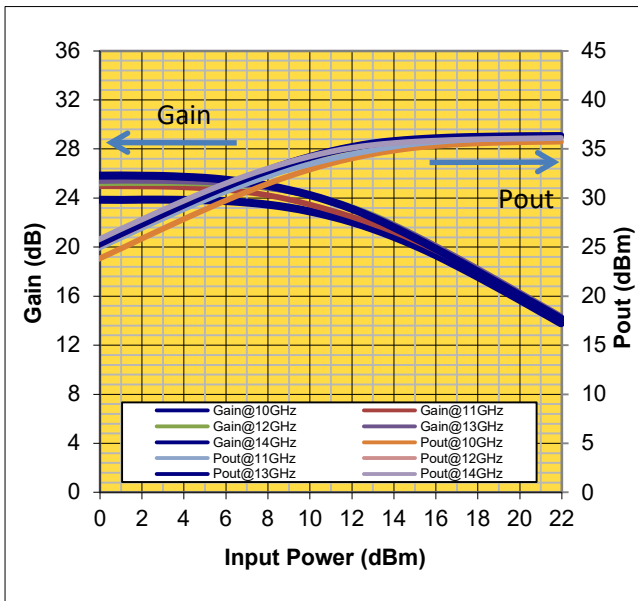
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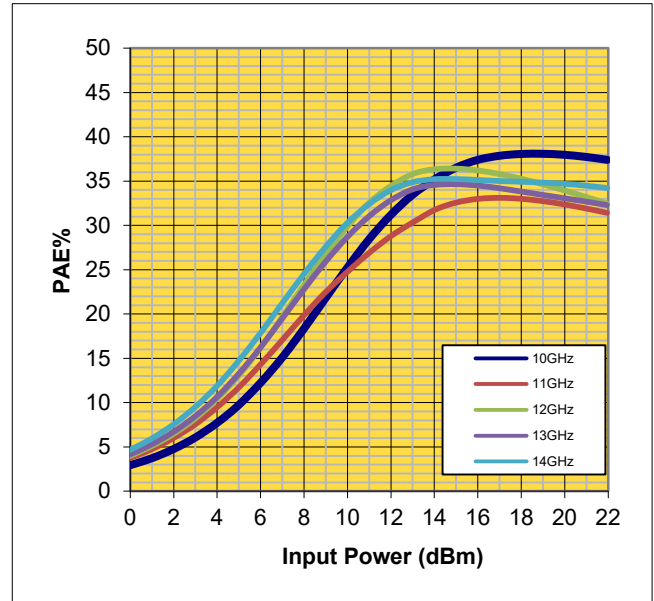


Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 18 V, Id1 = 80 mA, Id2 = 400 mA.

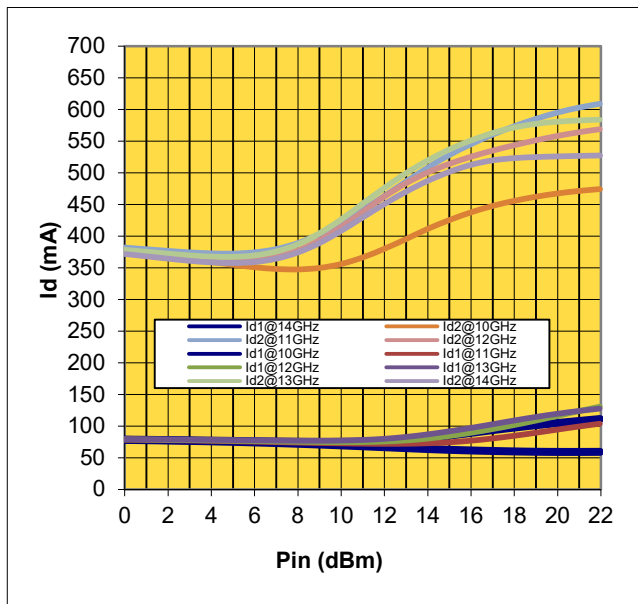
GAIN, Pout vs. Pin



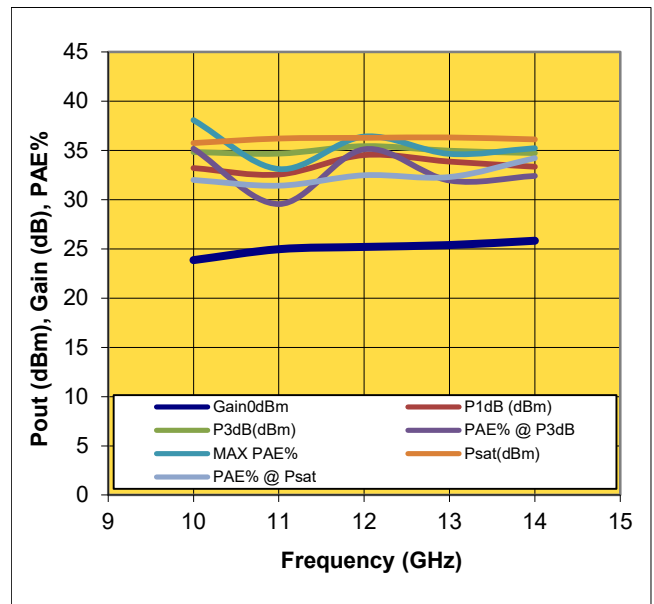
PAE vs. Pin



Id vs Pin



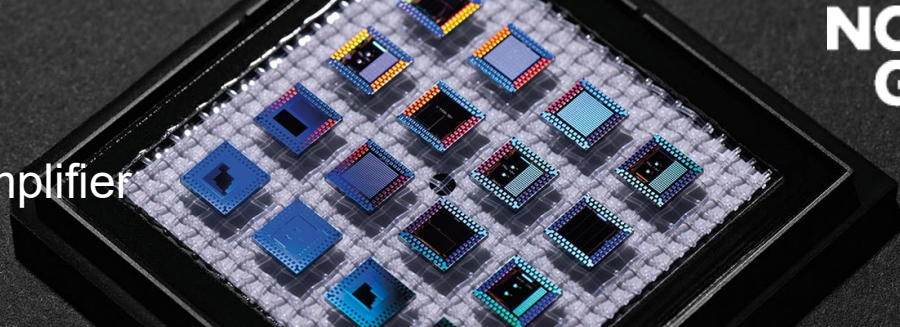
Pout, Gain, PAE vs. Frequency



** CW fixtured

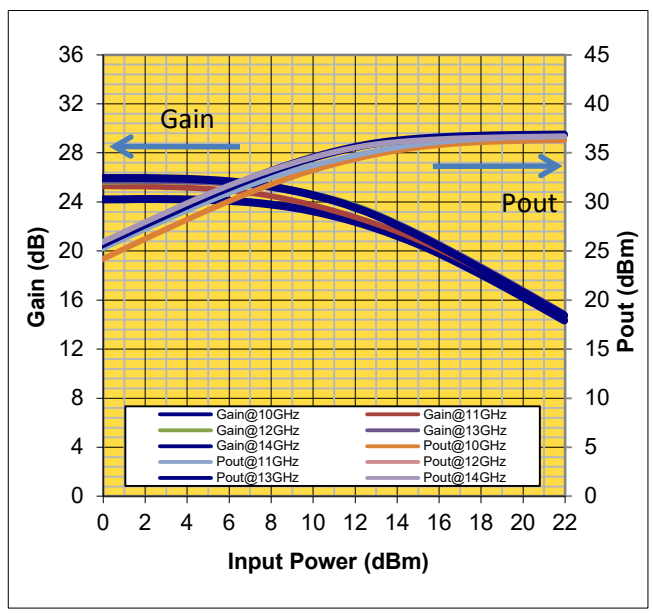
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APN252 10-14 GHz GaN Driver Amplifier

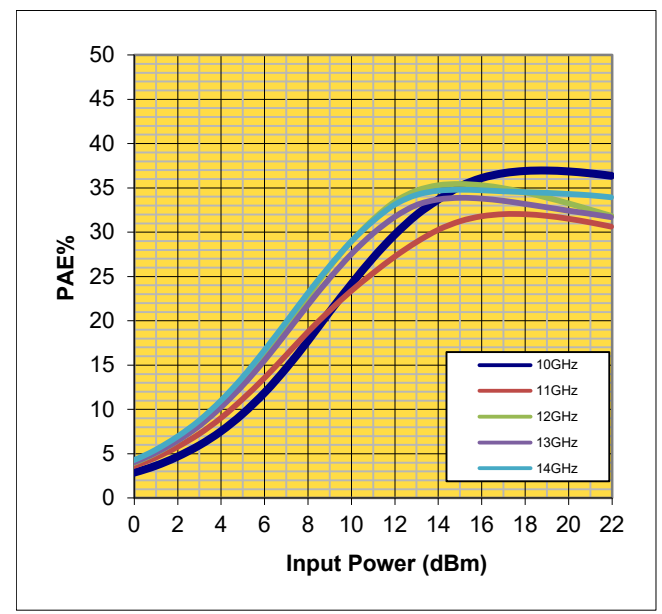


Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 20 V, Id1 = 80 mA, Id2 = 400 mA.

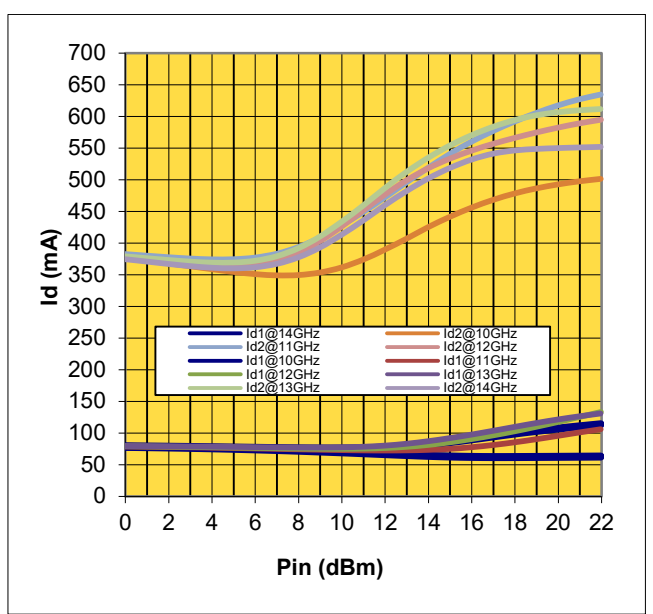
GAIN, Pout vs. Pin



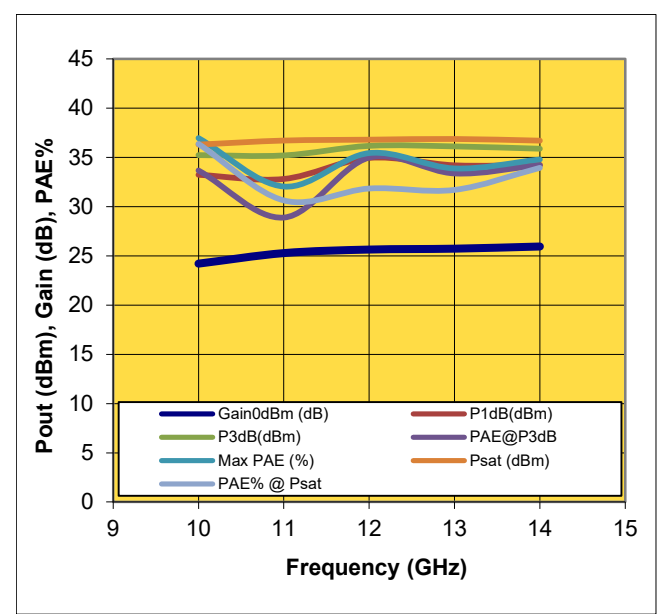
PAE vs. Pin



Id vs Pin



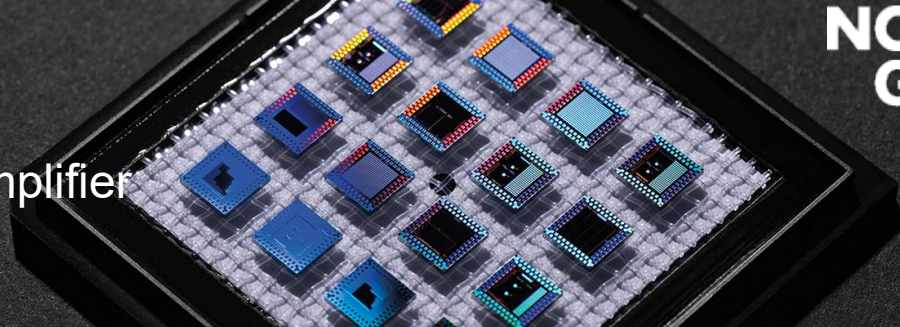
Pout, Gain, PAE vs. Frequency



** CW fixtured

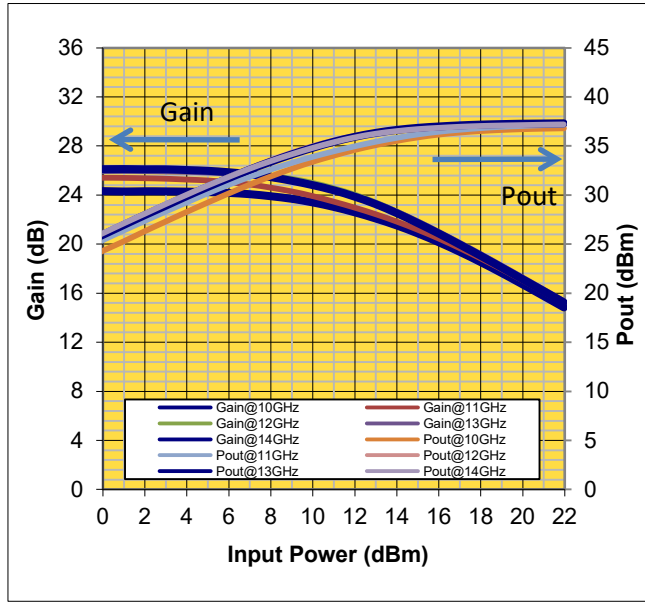
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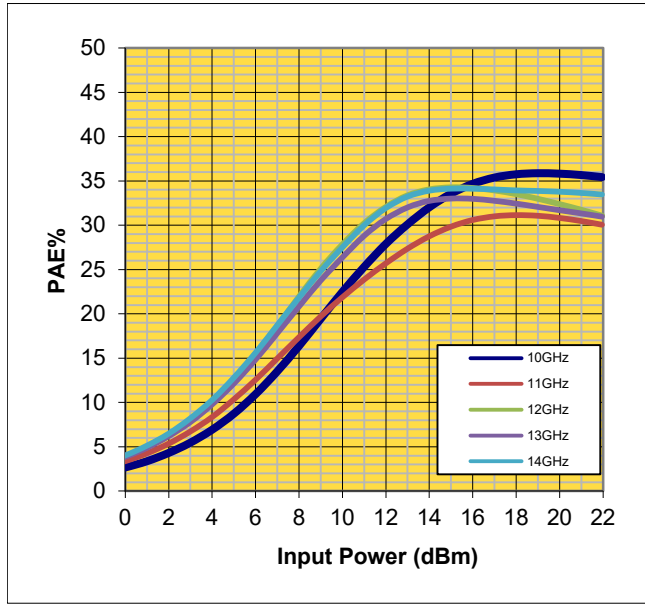


Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 80 mA, Id2 = 400 mA.

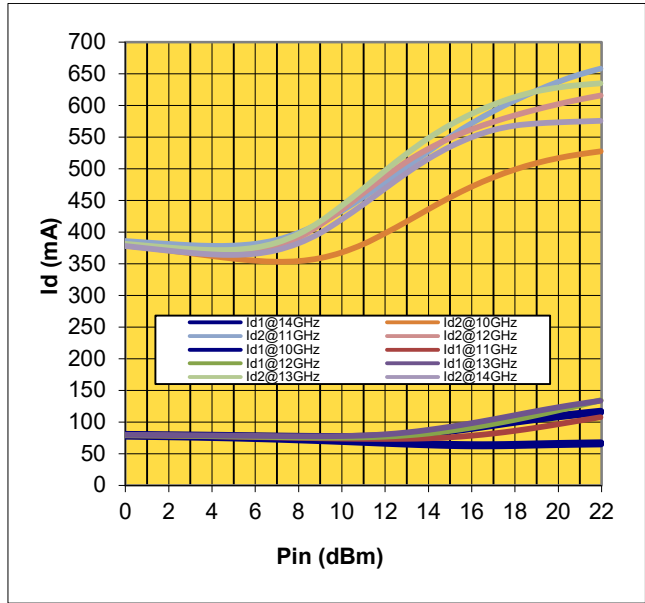
GAIN, Pout vs. Pin



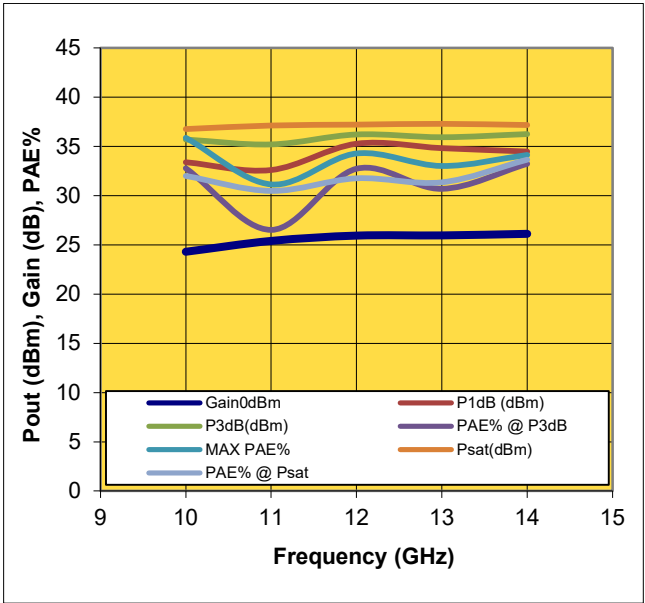
PAE vs. Pin



Id vs Pin



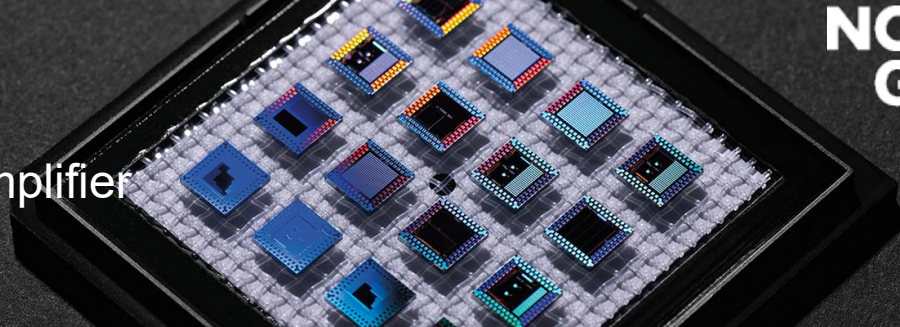
Pout, Gain, PAE vs. Frequency



** CW fixtured

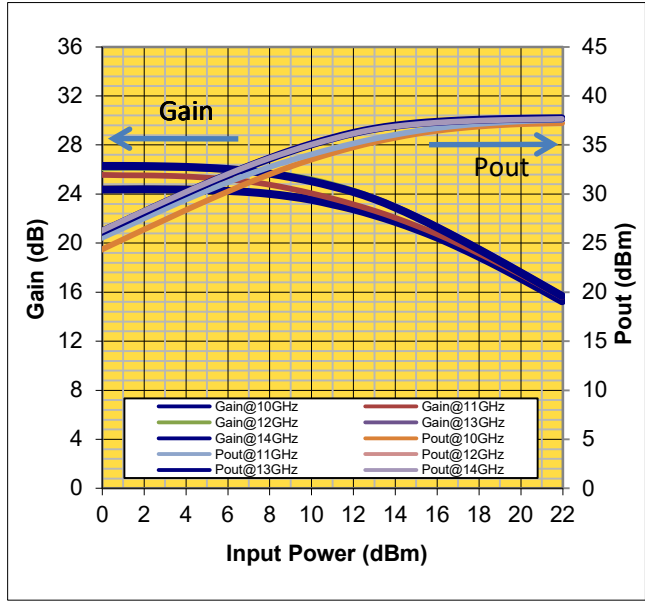
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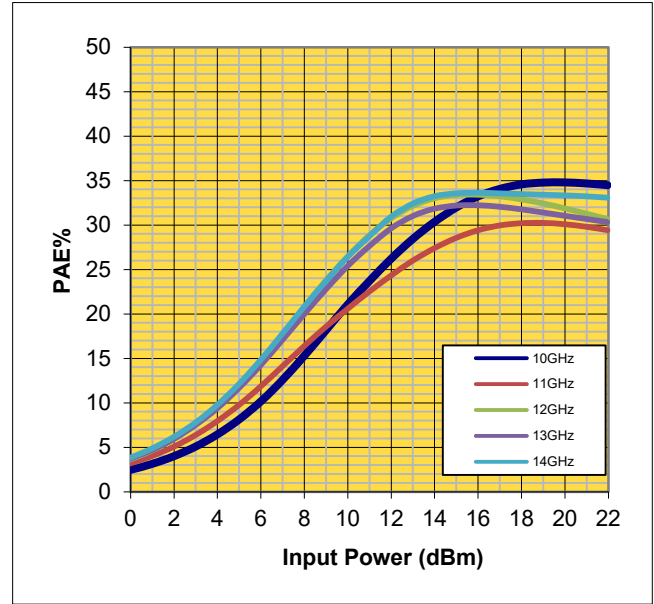


Measured Fixtured Performance Characteristics (Typical Performance at 25°C) Vd1 = Vd2 = 24 V, Id1 = 80 mA, Id2 = 400 mA.

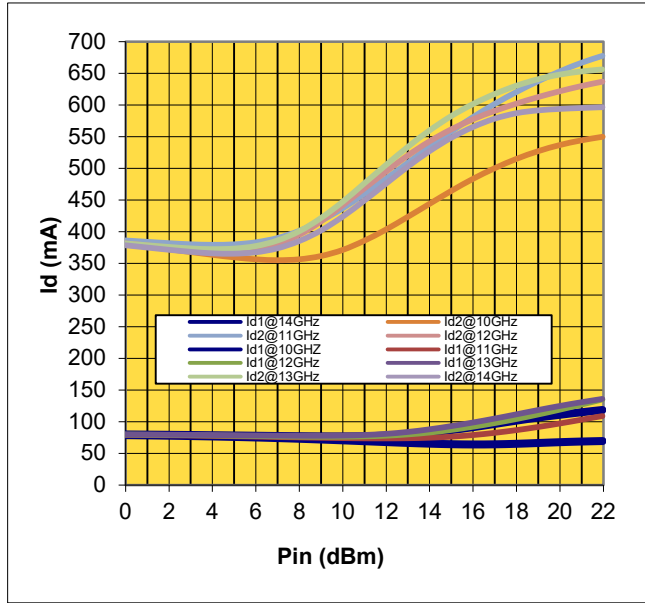
GAIN, Pout vs. Pin



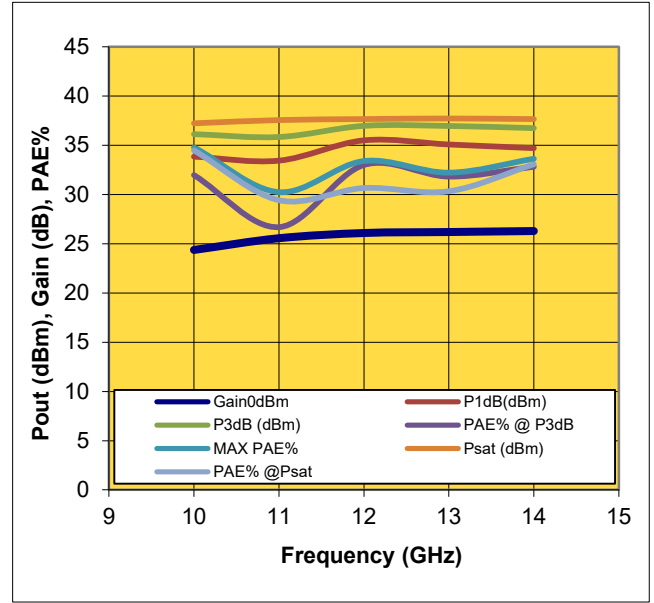
PAE vs. Pin



Id vs Pin



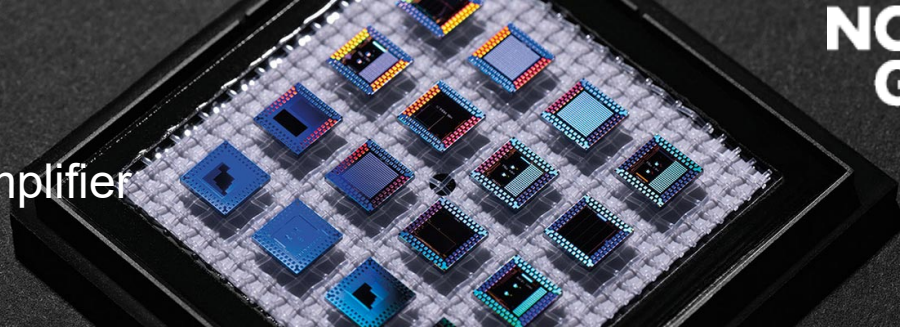
Pout, Gain, PAE vs. Frequency



** CW fixtured

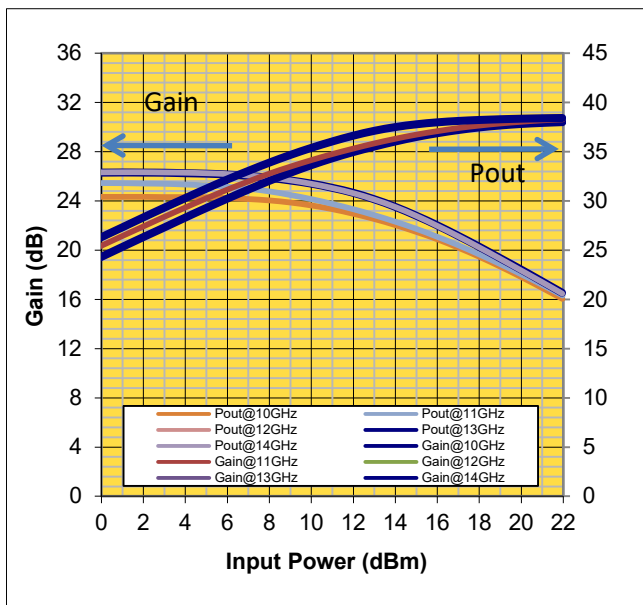
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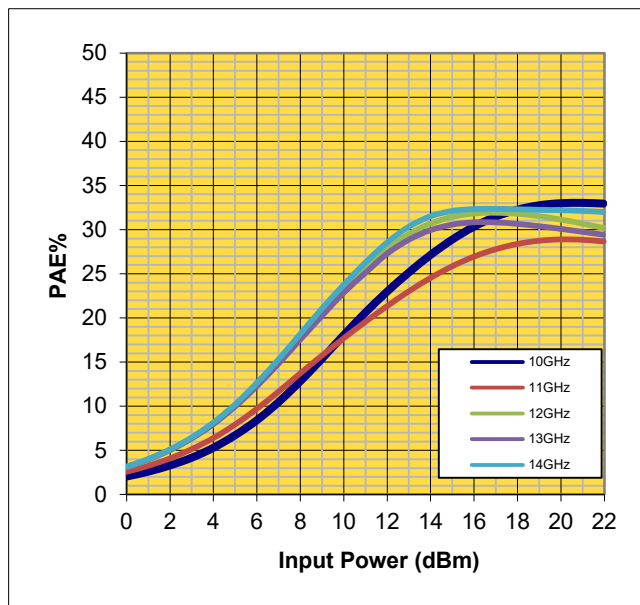


Measured Fixtured Performance Characteristics (Typical Performance at 25°C)
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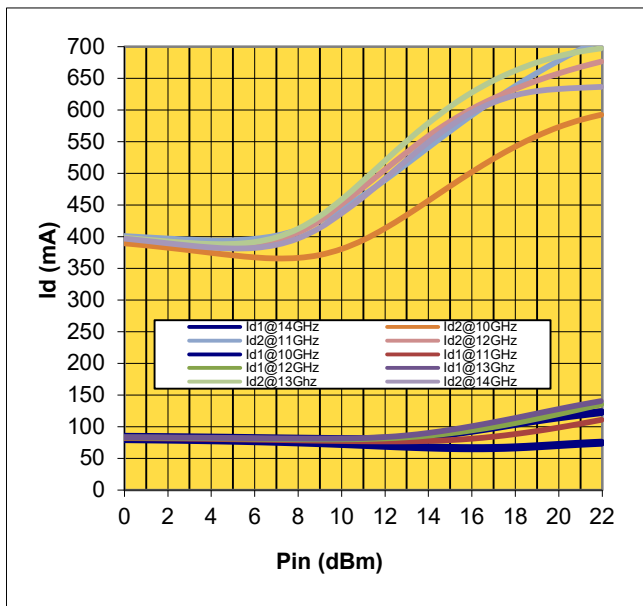
GAIN, Pout vs. Pin



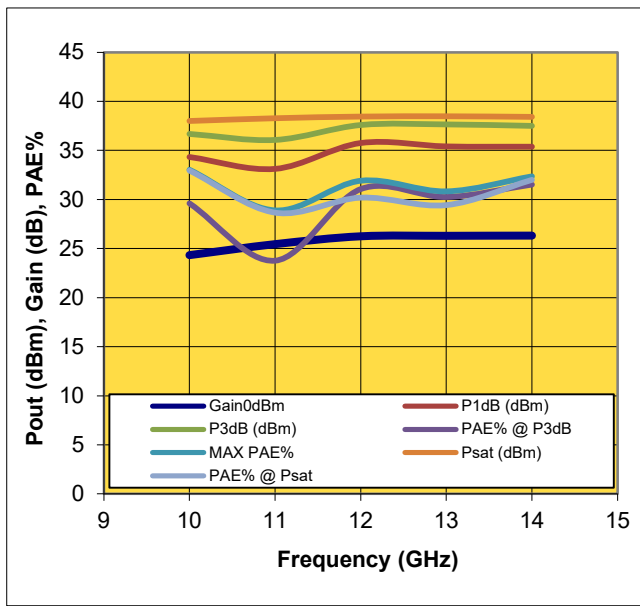
PAE vs. Pin



Id vs Pin



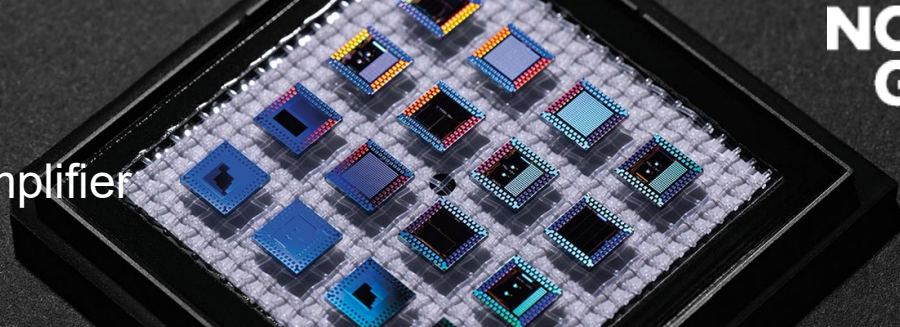
Pout, Gain, PAE vs. Frequency



** CW fixtured

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APN252
10-14 GHz
GaN Driver Amplifier

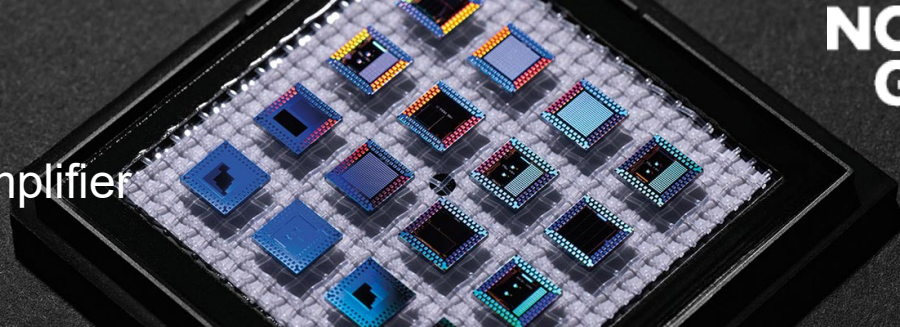


On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1 = Vd2 = 22 V, Id1 = 80 mA, Id2 = 400 mA. *

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
2.0	0.899	-27.894	0.011	-13.191	0.003	-74.296	0.913	-127.169
2.5	0.897	-34.450	0.007	29.924	0.006	67.173	0.901	-142.102
3.0	0.880	-41.418	0.011	76.199	0.003	159.887	0.905	-154.317
3.5	0.878	-47.188	0.015	73.819	0.002	58.033	0.888	-164.620
4.0	0.858	-54.658	0.026	91.709	0.004	-2.473	0.888	-174.073
4.5	0.854	-62.404	0.036	84.788	0.002	100.322	0.888	177.357
5.0	0.835	-69.960	0.070	85.619	0.001	120.852	0.863	168.433
5.5	0.817	-78.793	0.116	74.837	0.001	178.353	0.849	160.137
6.0	0.791	-88.398	0.189	61.545	0.004	-118.693	0.831	150.250
6.5	0.742	-97.439	0.280	48.412	0.002	-61.119	0.808	138.959
7.0	0.697	-108.546	0.427	41.136	0.000	-14.911	0.759	124.819
7.5	0.634	-120.022	0.739	33.414	0.000	48.197	0.687	106.795
8.0	0.553	-132.145	1.495	21.777	0.002	71.574	0.557	77.502
8.5	0.479	-146.318	3.408	-2.567	0.001	124.011	0.381	21.463
9.0	0.401	-160.805	7.529	-44.702	0.004	95.881	0.403	-82.633
9.5	0.301	-175.626	13.011	-99.394	0.008	97.065	0.585	-151.408
10.0	0.227	158.553	16.828	-155.933	0.008	56.173	0.591	176.839
10.5	0.155	119.267	18.023	155.495	0.006	9.692	0.661	160.191
11.0	0.108	69.035	19.036	113.078	0.007	-36.944	0.779	139.108
11.5	0.129	25.851	19.413	72.662	0.008	-86.203	0.819	107.327
12.0	0.134	-21.304	21.026	33.787	0.006	-137.814	0.753	76.519
12.5	0.142	-26.490	20.516	-6.140	0.008	-170.137	0.669	40.400
13.0	0.120	-57.406	20.425	-45.415	0.011	166.912	0.486	8.223
13.5	0.103	-62.790	19.867	-80.889	0.009	108.436	0.407	-8.863
14.0	0.111	169.101	20.901	-127.113	0.014	71.791	0.403	-9.839
14.5	0.294	82.837	17.677	-176.940	0.011	21.388	0.662	-29.754
15.0	0.463	41.556	11.663	135.892	0.009	-12.500	0.795	-57.869
15.5	0.542	14.637	7.156	101.842	0.005	-31.995	0.844	-80.318
16.0	0.558	-3.870	4.651	76.351	0.009	-37.761	0.853	-96.204
16.5	0.574	-15.110	3.114	55.293	0.005	-95.767	0.858	-108.506
17.0	0.578	-23.612	2.208	37.284	0.003	-108.928	0.851	-117.480
17.5	0.593	-30.657	1.620	20.764	0.003	-137.627	0.855	-125.183
18.0	0.598	-37.163	1.259	4.457	0.003	162.364	0.879	-131.837

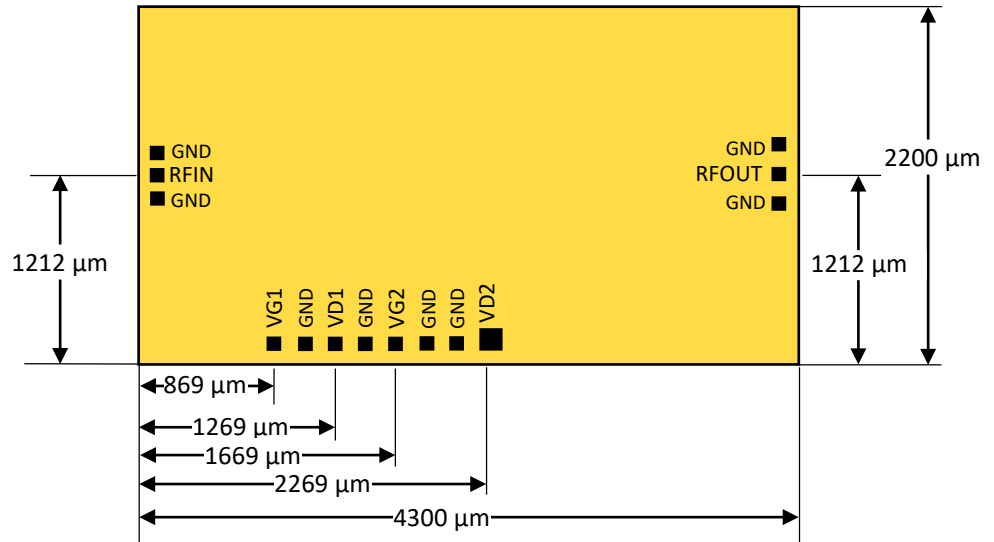
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APN252
10-14 GHz
GaN Driver Amplifier



Die Size and Bond Pad Locations (Not to Scale)

- X = 4300 ± 25 μm
- Y = 2200 ± 25 μm
- DC Bond Pad = 100 x 100 ± 0.5 μm
- VD2 DC Bond Pad = 140 x 140 ± 0.5 μm
- RF Bond Pad = 100 x 100 ± 0.5 μm
- Chip Thickness = 101 ± 5 μm



Biasing/De-Biasing Details:

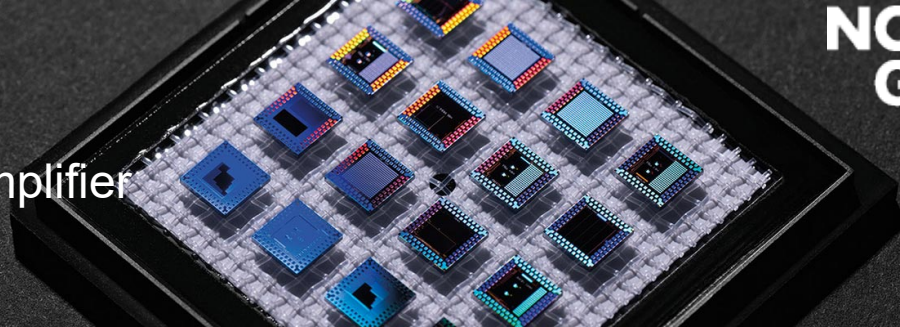
APN252 can be biased only from the top of the die.

Listed below are some guidelines for GaN device testing and wire bonding:



- a. Limit positive gate bias (G-S or G-D) to < 1V
- b. Know your devices' breakdown voltages
- c. Use a power supply with both voltage and current limit.
- d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
 - i. Apply negative gate voltage (-5 V) to ensure that all devices are off
 - ii. Ramp up drain bias to ~10 V
 - iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
 - iv. Ramp up drain to operating bias
 - v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
- e. Repeat bias procedure for each amplifier stage
- f. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
 - i. Gradually decrease drain bias to 0 V.
 - ii. Gradually decrease gate bias to 0 V.
 - iii. Turn off supply voltages
- g. Repeat de-bias procedure for each amplifier stage

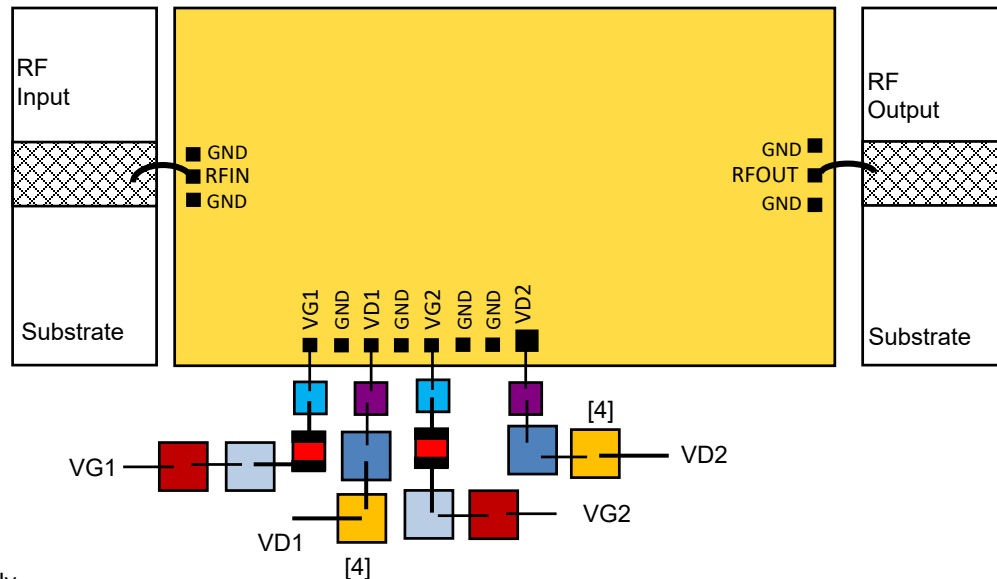
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APN252 10-14 GHz GaN Driver Amplifier



Suggested Bonding Arrangement

-  = 0.1uF, 50V (Shunt) [4]
-  = 0.01uF, 50V (Shunt)
-  = 100 pF, 50V (Shunt)
-  = 0.1uF, 15V (Shunt)
-  = 0.01uF, 15V (Shunt)
-  = 10 Ohms, 30V (Series)
-  = 100 pF, 15V (Shunt)



Note: APN252 can be biased only from the top of the die.

Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF, 50V Capacitors.

Mounting Processes

Most Northrop Grumman Aerospace Systems (NGAS) GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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