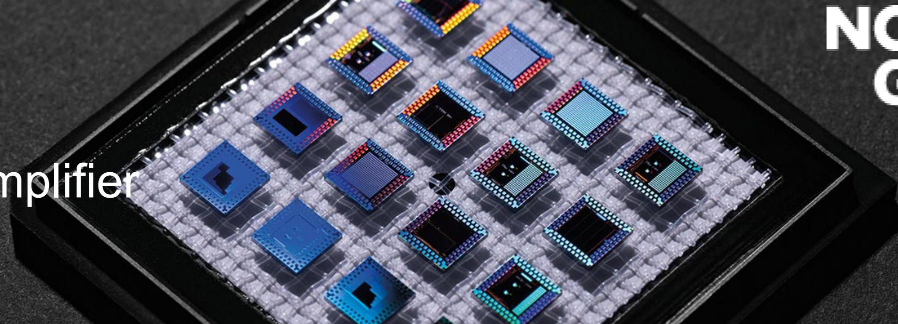
APN293
16-20.8 GHz
GaN Power Amplifier



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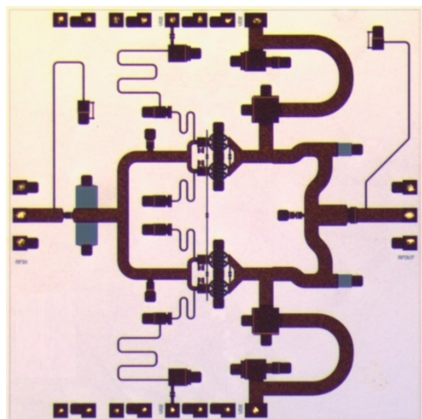

X = 3 mm Y = 3 mm

Product Features

- RF frequency: 16 to 20.8 GHz
- Linear Gain: 10 dB typ.
- Psat: 39 dBm typ.
- Efficiency @ P3dB > 40 %
- Die size = 9 sq. Mm
- 0.2um GaN HEMT
- 4 mil SiC substrate
- DC Power: 20 VDC @ 256 mA

Export Information
ECCN: **5A991.g**
HTS (Schedule B) code: **8542.33.0000**

Applications

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

Product Description

The APN293 monolithic GaN HEMT amplifier is a broadband, one-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, and Radar Applications. To support rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	16		14	GHz
Linear Gain	9	10		dB
Input Return Loss	7	14		dB
Output Return Loss	14	17		dB
P1dB		36		dBm
Psat		38.5		dBm
PAE @ Psat		30		%
Vd1, Vd2		20		V
Vg1		-3.5		V
Vg2		-3.5		V
Id1		144		V
Id2		400		mA

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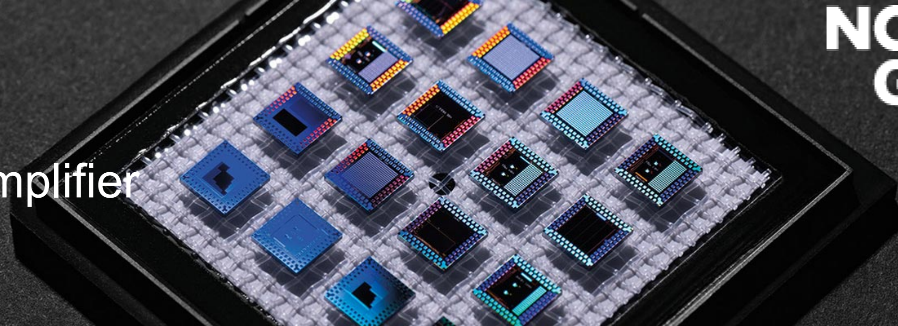
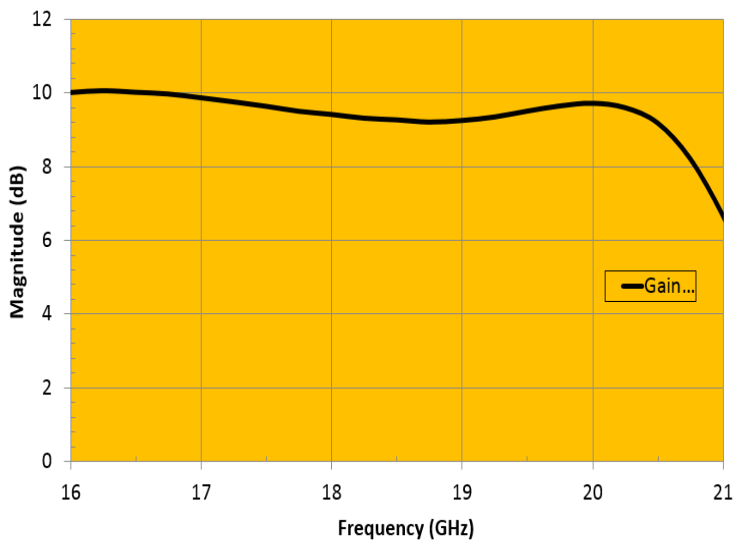
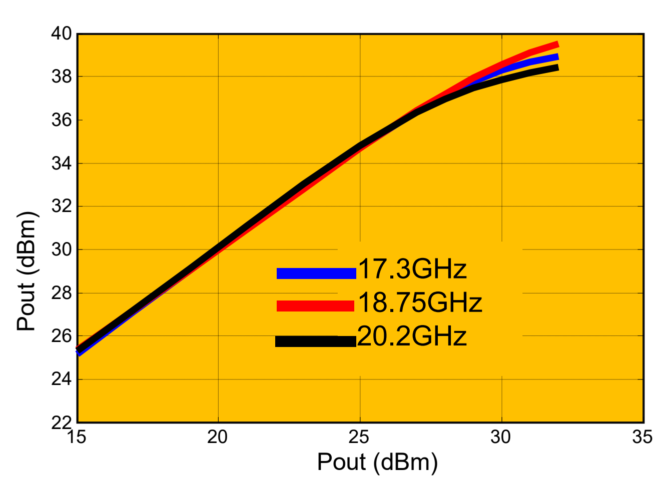


On-wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 20 V, Id1 = 144 mA, Id2= 400 mA.*

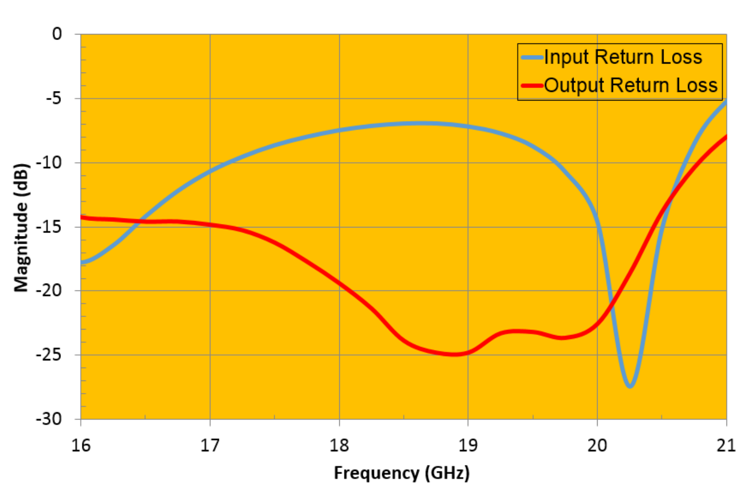
GAIN vs. Frequency



PAE, GAIN, Pout vs. Frequency



Input and Output Return Loss vs. Frequency



*Pulsed-power on-wafer

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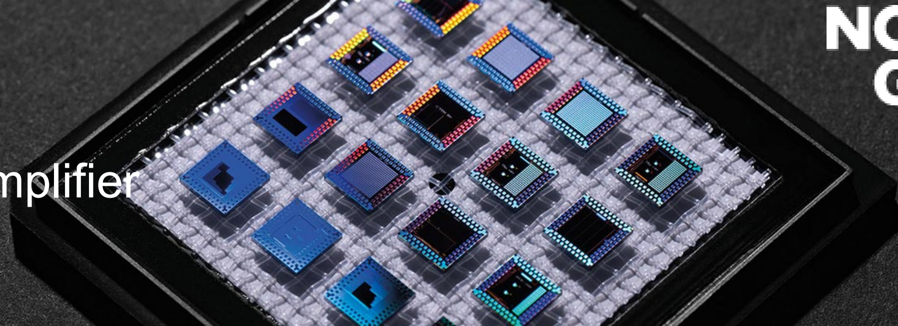
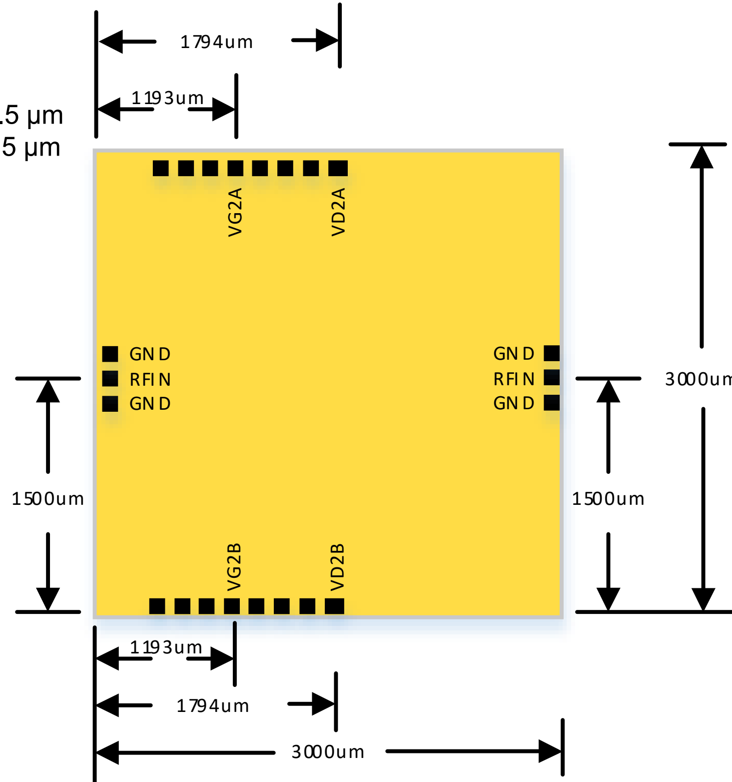


Die Size and Bond Pad Locations (Not to Scale)

X = 3000 µm ± 25 µm
Y = 3000 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:
Bias is single sided and is from the top only.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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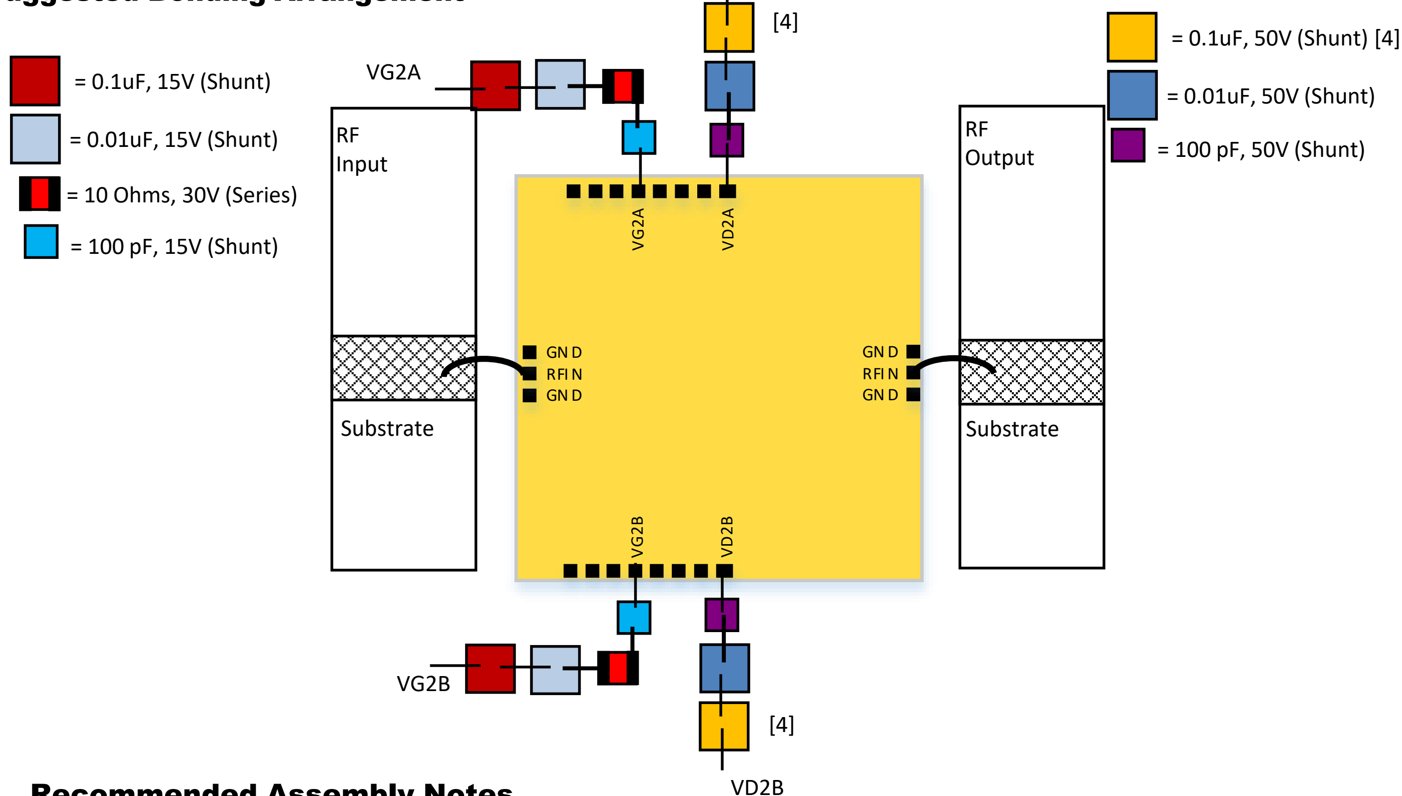
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGSC GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSC recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGSC parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO NGSC "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS.

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Page 4