Product Features

- RF frequency: 9 to 13.2 GHz
- Linear gain: >12 dB, typical
- OP1dB: 39 dBm, typical
- Psat: 41 dBm, typical
- PAE: >43% @ Psat
- Unconditionally stable
- DC Power: 20 Vdc at 768 mA
- Size: 5200 um x 4200 um
- Technology: 0.20 um GaN HEMT

Product Description

The APN294 monolithic GaN HEMT amplifier is a broadband, one-stage power device, designed for use in Point-to-Point and Multipoint Digital Radios, and Radar Applications. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Applications

- Military SatCom
- Phased-Array Radar Applications
- Point-to-Point Radio
- Point-to-Multipoint Communications
- Terminal Amplifiers

Performance Characteristics (Ta = 25°C)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>9</td>
<td>10</td>
<td>13.2</td>
<td>GHz</td>
</tr>
<tr>
<td>Linear Gain</td>
<td>10</td>
<td>12</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>15</td>
<td>15</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>15</td>
<td>15</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>P1db</td>
<td>39</td>
<td>39</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Psat</td>
<td>39</td>
<td>41</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>PAE @ Psat</td>
<td>41</td>
<td>41</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>Vd1, Vd2</td>
<td>20</td>
<td>20</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Vg1</td>
<td>-3.5</td>
<td>-3.5</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Vg2</td>
<td>-3.5</td>
<td>-3.5</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Id1</td>
<td>256</td>
<td>256</td>
<td>-</td>
<td>mA</td>
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</table>

Maximum SOA Ratings (Ta = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Max</th>
<th>Unit</th>
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<tr>
<td>DC Power</td>
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<td>28</td>
<td>W/mm</td>
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<tr>
<td>Vd1, Vd2</td>
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<td>28</td>
<td>V</td>
</tr>
<tr>
<td>Id1</td>
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<td>0</td>
<td>mA</td>
</tr>
<tr>
<td>Vg1, Vg2</td>
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<td>0</td>
<td>V</td>
</tr>
<tr>
<td>Assy. Temperature</td>
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<td>300</td>
<td>deg. C</td>
</tr>
</tbody>
</table>
Measured Performance Characteristics (Typical Performance at 25°C)
$V_d = 20.0 \, V$, $I_d1 = 250mA$

* Pulsed-Power On-Wafer
**Die Size and Bond Pad Locations (Not to Scale)**

\[
\begin{align*}
X &= 5200 \, \mu\text{m} \pm 25 \, \mu\text{m} \\
Y &= 420 \pm 25 \, \mu\text{m} \\
\text{DC Bond Pad} &= 100 \times 100 \pm 0.5 \, \mu\text{m} \\
\text{RF Bond Pad} &= 100 \times 100 \pm 0.5 \, \mu\text{m} \\
\text{Chip Thickness} &= 101 \pm 5 \, \mu\text{m}
\end{align*}
\]

**Biasing/De-Biasing Details:**
Bias is single sided and is from the top only.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V  
b. Know your devices’ breakdown voltages  
c. Use a power supply with both voltage and current limit.  
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.  
   i. Apply negative gate voltage (-5 V) to ensure that all devices are off  
   ii. Ramp up drain bias to ~10 V  
   iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved  
   iv. Ramp up drain to operating bias  
   v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved  

e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):  
   i. Gradually decrease drain bias to 0 V.  
   ii. Gradually decrease gate bias to 0 V.  
   iii. Turn off supply voltages  

f. Repeat de-bias procedure for each amplifier stage
Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do NOT use the 0.1uF, 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!