**Product Features**

- RF frequency: 47.2 to 51.4 GHz
- Linear Gain: 15-18 dB across the band.
- Psat: 10-12 Watt across the band
- Die Size: 6.4 mm²
- 0.15um GaN HEMT Process
- 3 mil SiC substrate
- DC Power: 28 VDC @ 1.62 A

**Applications**

- 5G Wireless
- Internet of Things (IoT)
- SatCom Terminals

**Product Description**

The APN318 GaN HEMT Power/Driver amplifier is a three-stage Single-ended power device, designed for use in 5G wireless and SatCom Terminals. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

**Performance Characteristics (Ta = 25°C)**

<table>
<thead>
<tr>
<th>Specification *</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>47.2</td>
<td>15.5</td>
<td>51.4</td>
<td>GHz</td>
</tr>
<tr>
<td>Linear Gain</td>
<td>12</td>
<td>10</td>
<td>18</td>
<td>dB</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>8</td>
<td>10</td>
<td>10</td>
<td>dB</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>8</td>
<td>10</td>
<td>10</td>
<td>dB</td>
</tr>
<tr>
<td>Psat (PP*)</td>
<td>10</td>
<td>12</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>PAE @ Psat (PP*)</td>
<td>30</td>
<td>20</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Max PAE (PP*)</td>
<td>24</td>
<td>20</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Vd1=Vd1a=Vd2=Vd2a=Vd3=Vd3a</td>
<td>20</td>
<td>24</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>Vg1, Vg1a, Vg2, Vg2a, Vg3, Vg3a</td>
<td>-3.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Id1+Id1a</td>
<td>220</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Id2+Id12a</td>
<td>440</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Id3+Id3a</td>
<td>960</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

*Pulsed-Power On-Wafer unless otherwise noted

**Export Information**

ECCN: 5A991.g
HTS (Schedule B) code: 8542.33.0000

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**Preliminary Information:** The data contained in this document describes new products in the sampling or preproduction phase of development and is for information only. Northrop Grumman reserves the right to change without notice the characteristic data and other specifications as they apply to this product. The product represented by this datasheet is subject to U.S. Export Law as contained the EAR regulations.
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 220 mA, Id2 + Id2a = 440 mA, Id3 + Id3a = 960mA

*Gain: is limited by the frequency measurement capabilities
**Pin=26dB @[46-49]GHz; Pin=23dB @50GHz; Pin=13dB @51GHz
Fixture measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 220 mA, Id2 + Id2a = 440 mA, Id3 + Id3a = 960 mA
Die Size and Bond Pad Locations (Not to Scale)

X = 3200 μm ± 25 μm
Y = 2000 ± 25 μm
DC Bond Pad = 100 x 100 ± 0.5 μm
RF Bond Pad = 100 x 100 ± 0.5 μm
Chip Thickness = 101 ± 5 μm

Biasing/De-Biasing Details:
Bias for 1st must be from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices’ breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
   i. Apply negative gate voltage (-5 V) to ensure that all devices are off
   ii. Ramp up drain bias to ~10 V
   iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
   iv. Ramp up drain to operating bias
   v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved

e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
   i. Gradually decrease drain bias to 0 V.
   ii. Gradually decrease gate bias to 0 V.
   iii. Turn off supply voltages
**Recommended Assembly Notes**

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF, 50V Capacitors.

**Mounting Processes**

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

**Note:** Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

**CAUTION:** THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS. **PLEASE ALSO REFER TO OUR “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!**

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