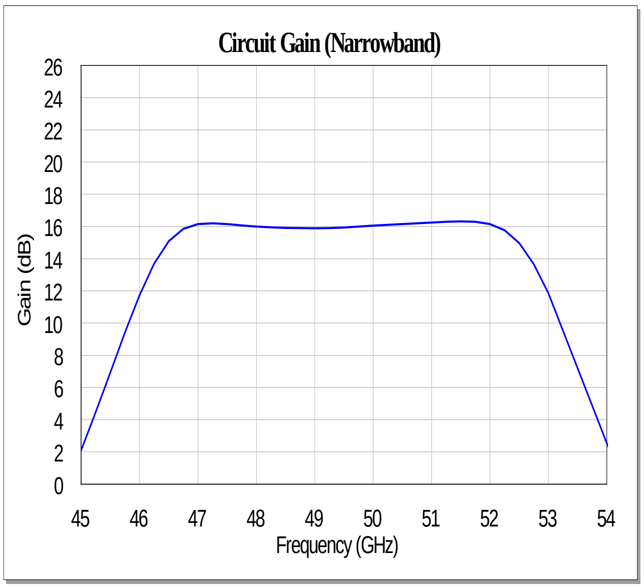
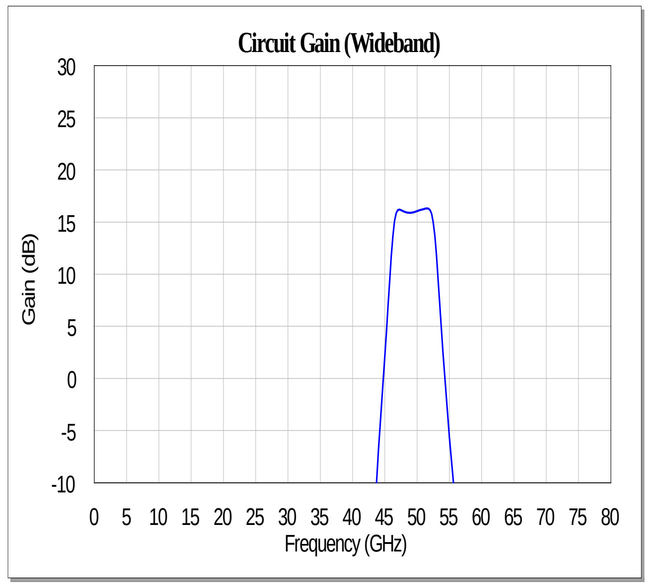
Simulated Performance Characteristics (Typical Performance at 25°C)

Vd = 24.0 V, Id1 + Id1a = 220 mA, Id2 + Id2a = 440 mA, Id3 + Id3a = 960 mA

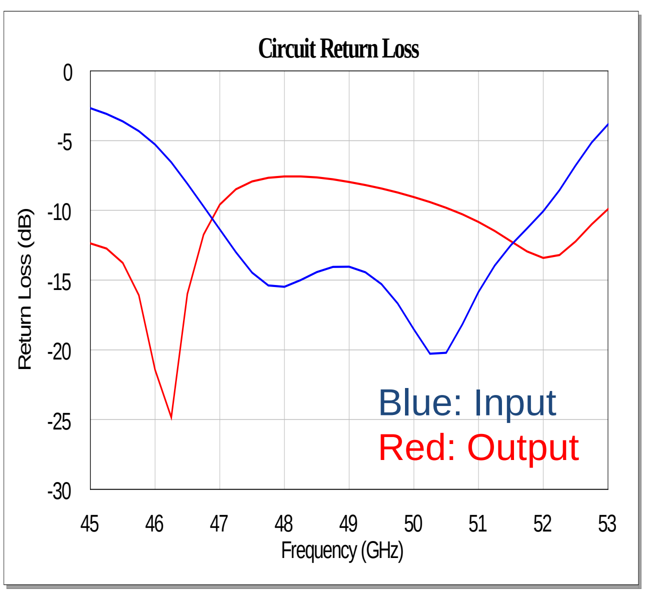
Circuit Gain vs. Frequency (Narrow Band)



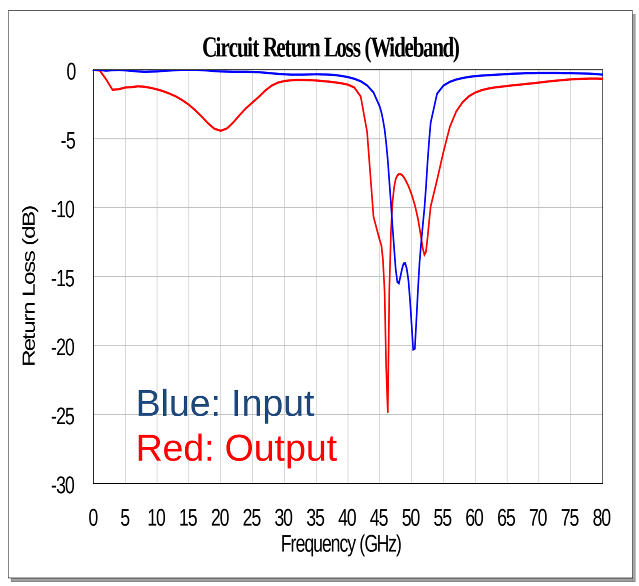
Circuit Gain vs. Frequency (Wide Band)

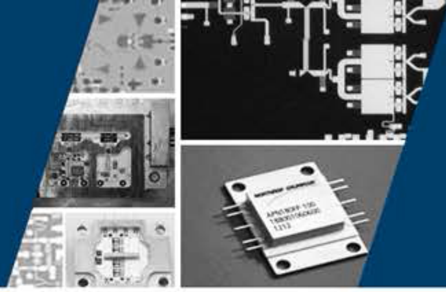


Return Loss vs. Frequency (Narrow Band)



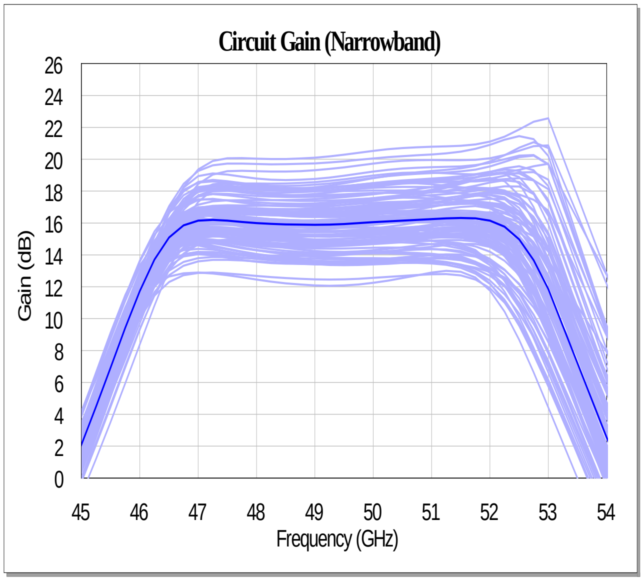
Return Loss vs. Frequency (Wide Band)



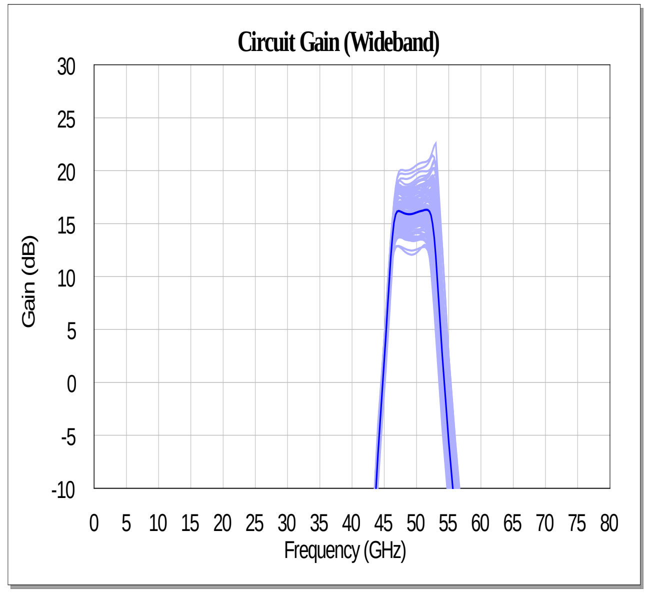


Simulated Performance Characteristics (Typical Performance at 25°C)
* Uncorrelated Monte Carlo for Distribution
Vd = 24.0 V, Id1 + Id1a = 220 mA, Id2 + Id2a = 440 mA, Id3 + Id3a = 960 mA

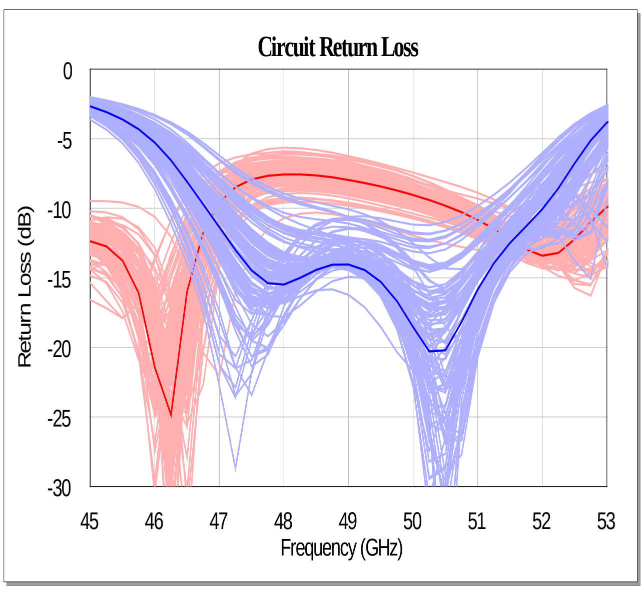
Circuit Gain vs. Frequency (Narrow Band)



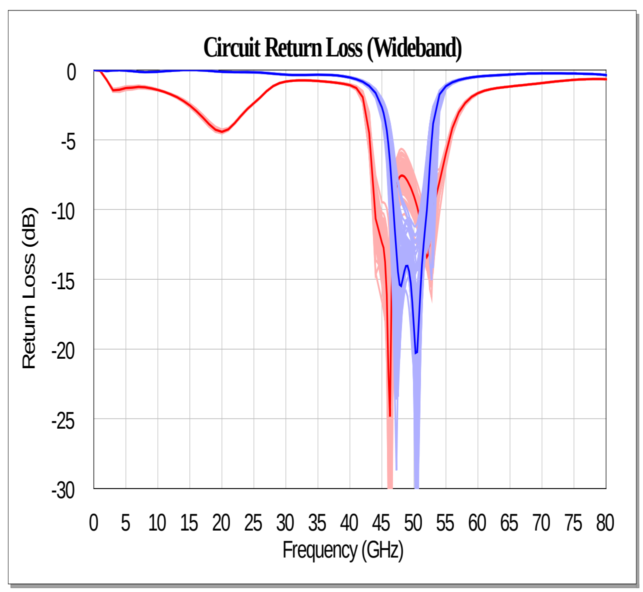
Circuit Gain vs. Frequency (Wide Band)



Return Loss vs. Frequency (Narrow Band)



Return Loss vs. Frequency (Wide Band)



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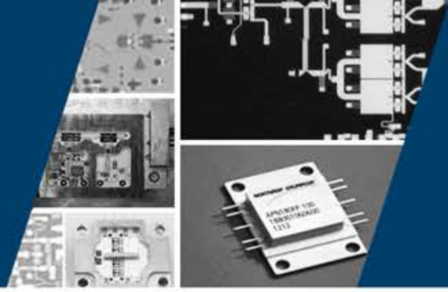
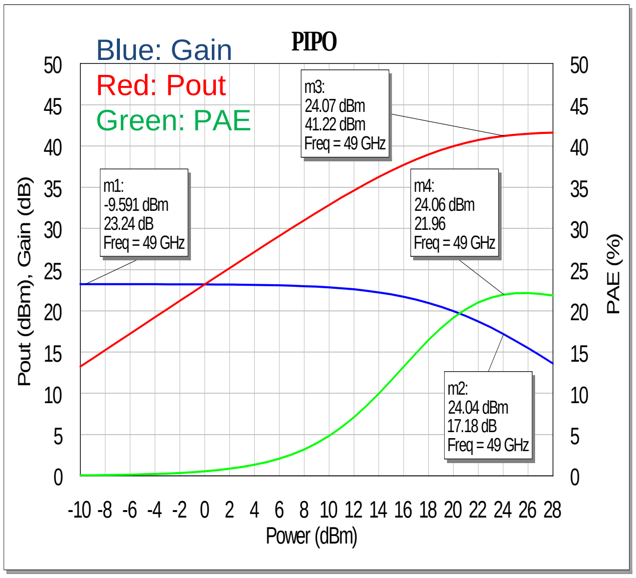
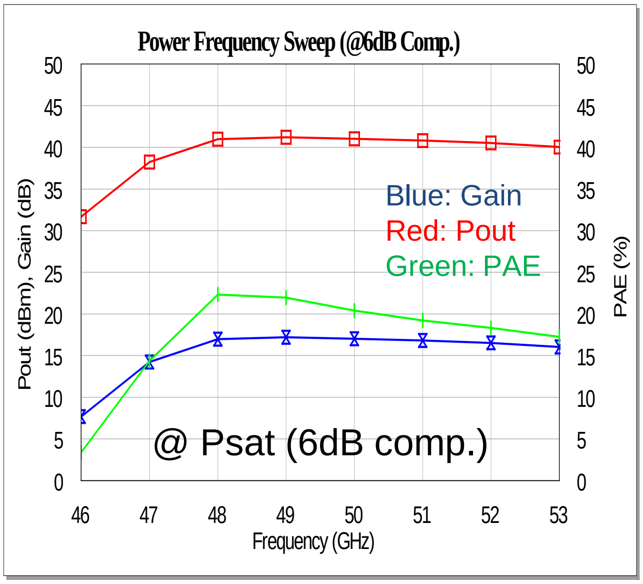


Simulated Power Performance Characteristics (Typical Performance at 25°C)
Vd = 24.0 V, Id1 + Id1a = 220 mA, Id2 + Id2a = 440 mA, Id3 + Id3a = 960 mA

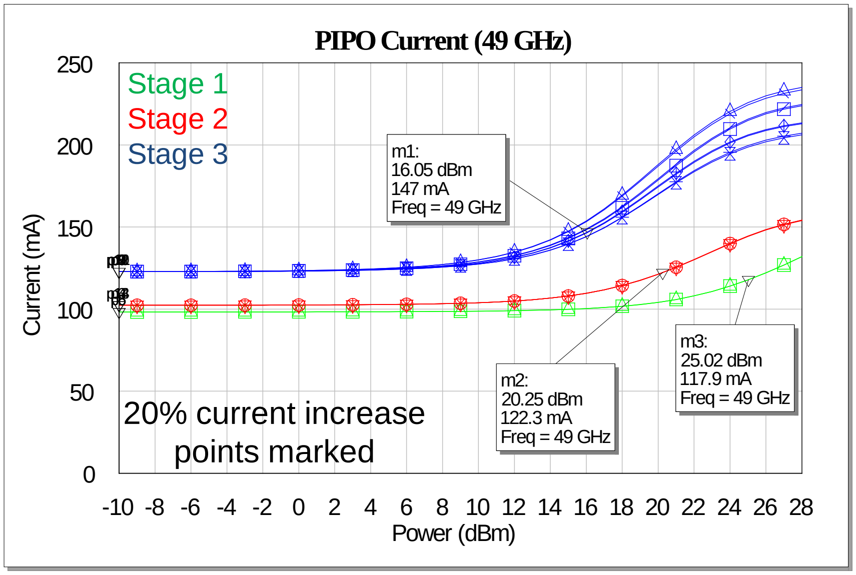
**Output Power vs. Input Power
Simulated Performance**



**Output Power and Gain vs. Frequency
Simulated Performance**



**Drain Current vs. Input Power
Simulated Performance**



Stages compress in order from last to first

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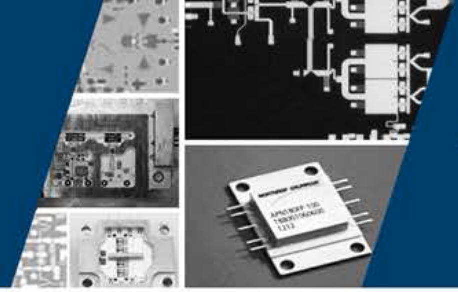
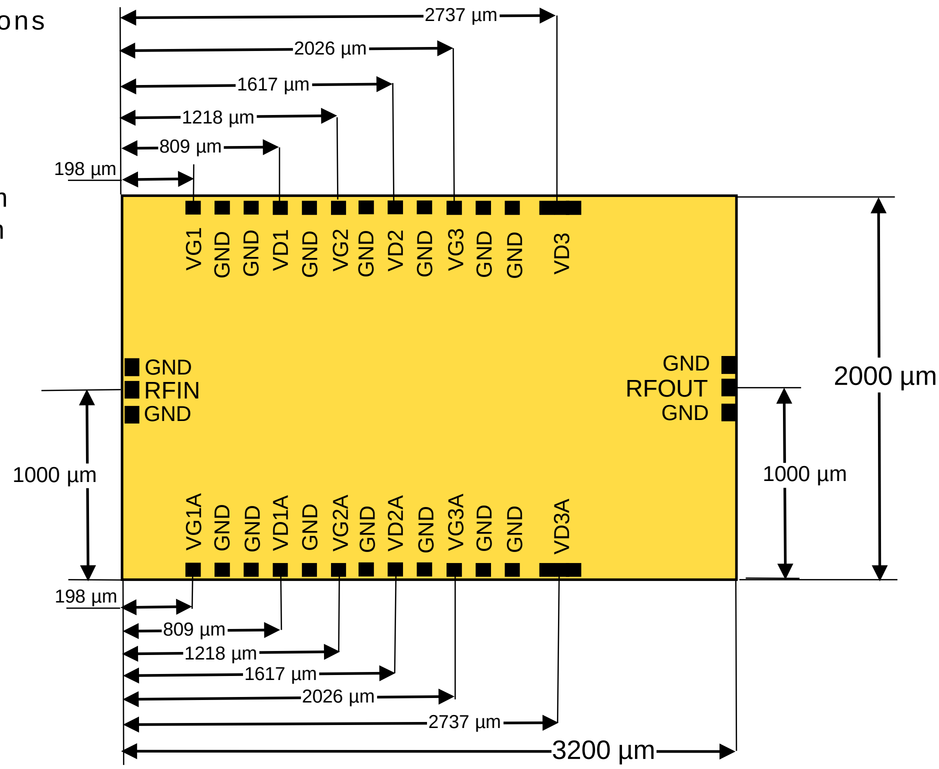


Die Size and Bond Pad Locations (Not to Scale)

X = 3200 µm ± 25 µm
Y = 2000 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm

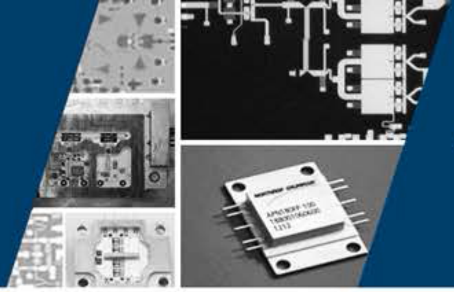


Biasing/De-Biasing Details:

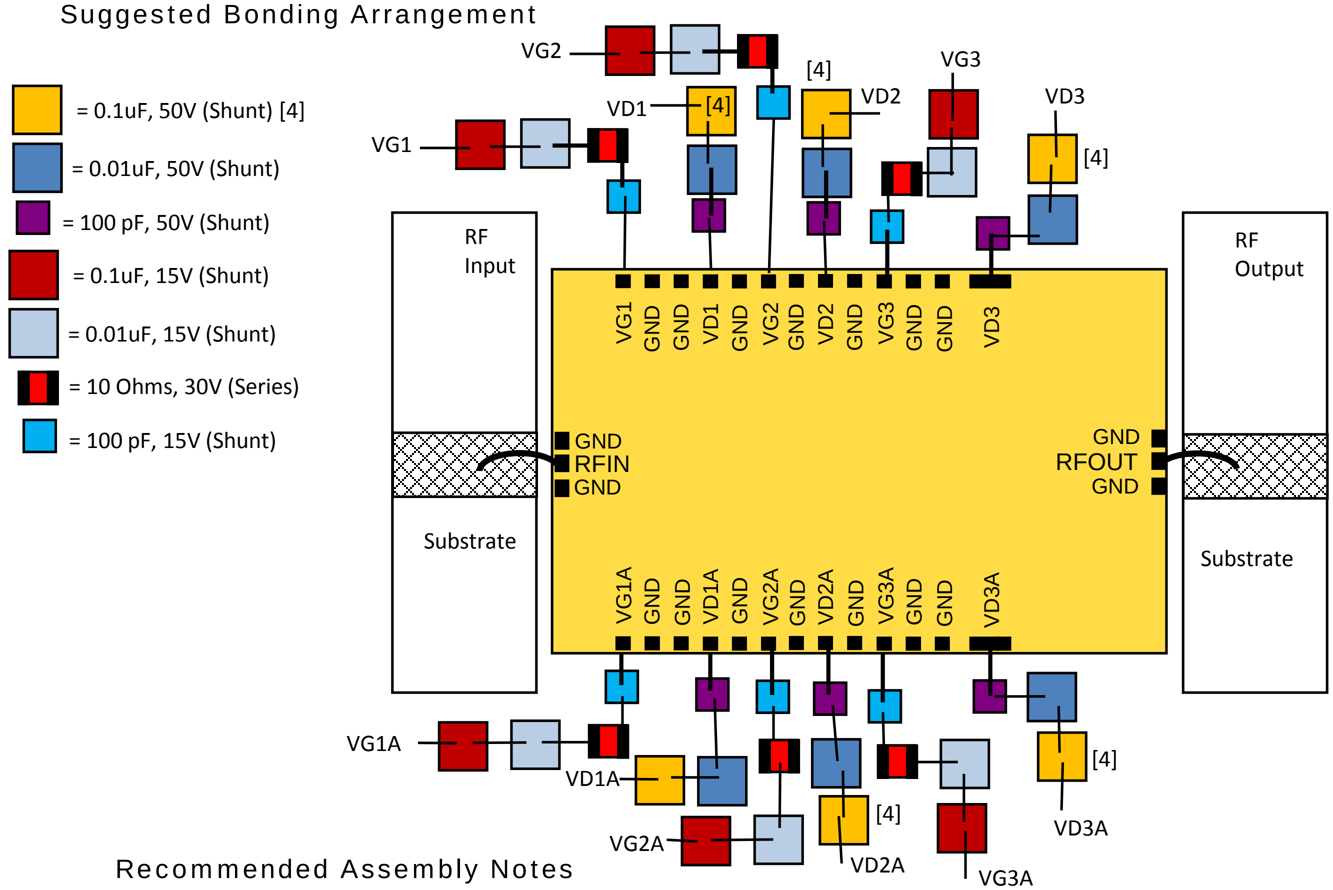
Bias for 1st must be from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages



Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320^{o}C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS. PLEASE ALSO REFER TO OUR “GaN Chip Handling Application Note” BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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