Application Note

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GaN IC Die Handling, Assembly and Testing Techniques

1. Scope

This document describes the storage and handling requirements for GaN IC chips. It also describes recommended assembly and testing techniques for users of GaN IC chips. Chips are usually delivered to the end user as individual chips stored in plastic chip trays or Gel-Pak. This document provides guidelines to aid the user in the assembly of GaN IC die in a manner consistent with desired electrical performance.

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1.1 Organization of Document

This document addresses the following areas:

- Packaging for shipment: Paragraph 3.1
- Allowable storage conditions: Paragraph 3.2
- Recommended assembly processes: Paragraph 3.3
- External Components: Paragraph 3.4
- Electrostatic discharge sensitivity (ESD): Paragraph 3.5
- General Testing Guidelines: Paragraph 3.6

2. Applicable Documents

The “MIL_STD_883, Test Methods and Procedures for Microelectronics” is referenced in this document.

3. Handling Requirements and Process Recommendations

3.1 Packaging for Shipment

GaN chips may be as thin as 4 mils (100 microns) at their thickest point. Due to this, it is necessary to treat GaN chips with care. Chips are packaged in Fluoroware (or equivalent) anti-static chip trays or Gel-Pak boxes. The container is wrapped in a shock absorbent material, such as bubble-pack prior to boxing the shipment.

3.2 Allowable Storage Conditions

Compared to many other microelectronic devices, GaN chips are relatively durable under a wide range of storage environments. NGAS's GaN ICs have no exposed materials that can easily corrode or degrade. All exposed metallizations are gold, and all active devices are passivated with silicon nitride. It is obviously essential that the storage environment be free of any substance that can degrade these materials. Long-term exposure to concentrated agents capable of corroding SiC or other metals is also not recommended, since the passivation layers are thin and not completely impervious.

3.2.1 Recommended Atmosphere

Although not necessary, a clean, dry nitrogen atmosphere is recommended for storage. Normal ambient air will not damage GaN devices, but if the chips are allowed to become wet or dirty, they will be difficult to clean.

3.2.2 Storage Temperatures

NGAS's GaN ICs are recommended to be stored at room temperature (25 3C). NGAS's GaN ICs can be stored at 125 C indefinitely without damage. GaN chips are capable of surviving much higher temperatures for shorter times.

3.3 Recommended Assembly Process

3.3.1 Individual Chip Handling

The metallization patterns on the frontside of the chip are very fragile. Any tool that contacts the frontside of the chip must be used with extreme caution. Vacuum pickup tools may be used on GaN chips, but NGAS recommends that the proper tool be used that minimizes contact with sensitive elements of the chip. Vacuum pickup tools that contact the backside of the chip, center of the chip, or edges of the chip should be selected to minimize contact to sensitive areas of the chip. Sensitive areas include airbridges, transistors, diodes, capacitors, and thin film resistors. If tweezers are used, it is recommended to use ESD compliant tweezers.
Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

Recommended procedures for preventing ESD damage are listed below:

- Adequately train personnel in the prevention of ESD damage before they handle GaN devices.
- Follow ESD prevention procedures throughout assembly and test. Use pin-to-case grounding, or pin shielding, or back bonding (see paragraph 3.3.4) whenever possible.
- Store GaN chips and wafers in anti-static containers. For chip trays, also known as waffle packs), NGAS recommends Fluoroware STAT-PRO 400 trays.
- Ensure that all equipment is properly grounded and isolated from each other.
- Handle GaN chips only at workstations properly equipped with ESD-prevention products and materials (e.g. grounded wrist straps, grounded table tops, etc.)

Table II. G-S damage threshold from Electrostatic Discharge

(MIL-STD-883, Method 3015)

Device	Damage Threshold Positive Polarity (V)	Damage Threshold Negative Polarity (V)
GaN 0.25/0.20 um Power-HEMT (device)	10*	> 80

* Failed at first 10V step.

3.6 General testing guidelines

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely debias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat debias procedure for each amplifier stage

Table III. Summary of NGAS's GaN IC Handling Recommendations

	Recommended Practice	Comments
Packaging Chips	Store in individual chip trays (Fluoroware, STAT-PRO 400, or equivalent).	
Storage General	Avoid exposure to corrosive materials.	Exposed surfaces (gold and silicon nitiride) are corrosion resistant, but still require careful handling.
Atmosphere	Store in dry nitrogen.	Normal air is not damaging, but care must be taken to avoid chips becoming wet or dirty.
Temperature	Store below 125C.	Chips can withstand higher temperatures for short periods of time.
Assembly Chip Handling	Use extreme caution with tools that contact the frontside of the chip.	Verify that any vacuum pick-up tool which contact the front of the chip do not cause damage, or only use tools against the backside of the chip.
Training	Personnel require training and practice to safely handle GaN chips.	Previous experiences with silicon IC chips or ceramic substrates does not qualify for GaN chips.
Mounting	Mount with conductive epoxy.	NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320oC for 30 seconds
Wire Bonding	Manual, wedge-wedge gold ribbon bond tool, with no flame-off feature. Employ back bonding where possible. Always check the voltage on the bonding tip with an oscilloscope before bonding.	Ball bonding is not recommended. Wire bonding equipment can generate dangerous voltages at the tip or stage. Monitor all bonding equipment regularly.
Electrostatic Discharge Protection	Follow recommendation in Paragraph 3.5	Treat all GaN IC chips as Class 0 ESD sensitive.